

Compal Confidential

V330/V530/EX3

DIS M/B Schematics Document

Intel Kabylake RU Processor with DDR4

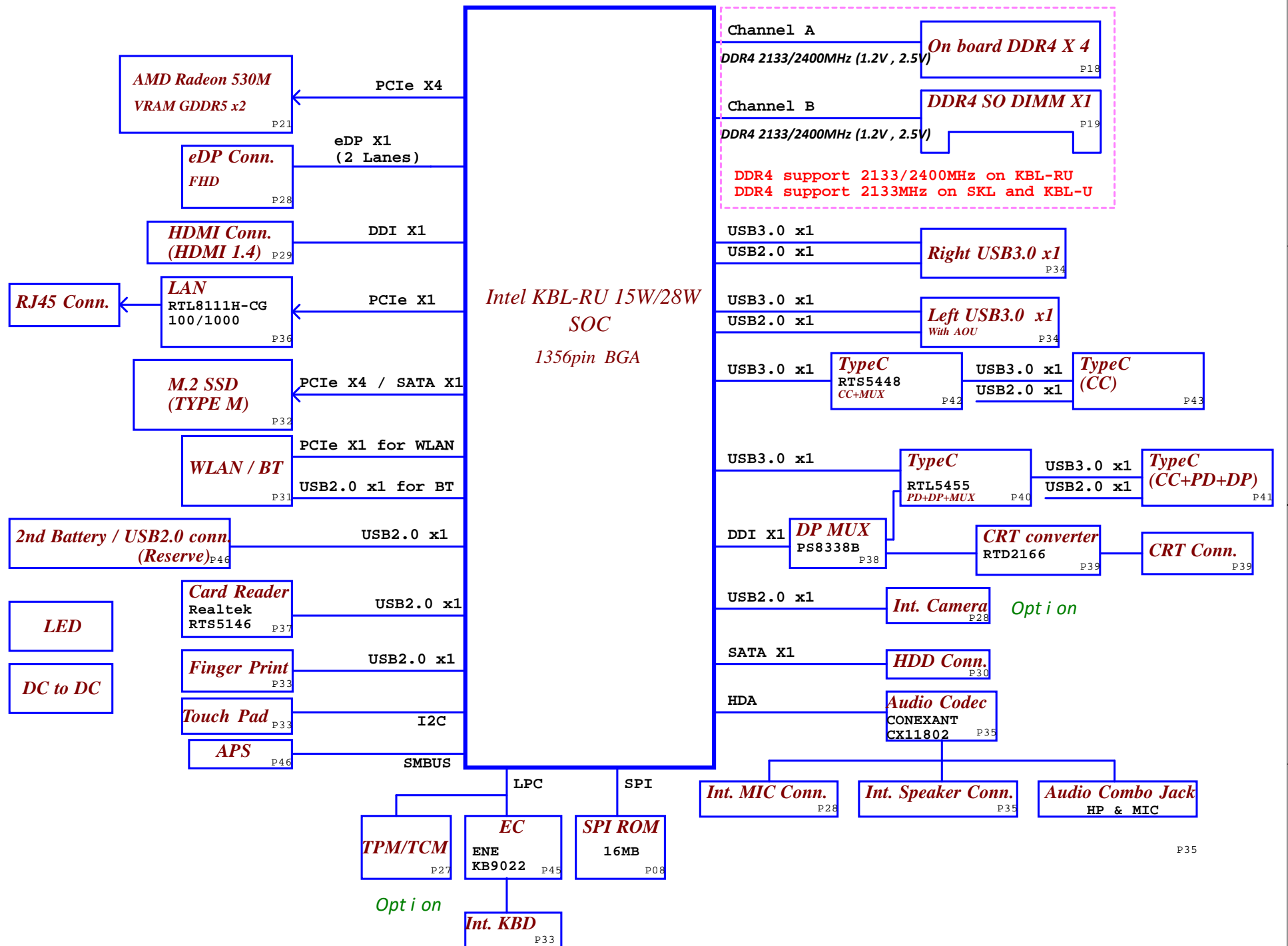
AMD R17M

2017-06-15

LA-F481P

REV : 0 . 2

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Issued Date		Deciphered Date		Title Cover Page		
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Voltage Rails

power plane	+RTCBATT	+B +5VL +3VL	+5VALW +3VALW +1.8VALW +1VALW	+1.0V_VCCST +2.5V +1.2V	+5VS +3VS +3VGS +1.8VGS +1.0VS_VCCIO +PCIE_VGS +VGA_CORE +1.35VS_VRAM +0.6VS +VCCCORE +VCCGT +VCCSA
State					
S0	O	O	O	O	O
S3	O	O	O	O	X
S5 and S4/AC	O	O	O	X	X
S5 and S4/Battery only	O	O	X	X	X
S5 and S4/AC&Battery don't exist(Only RTC)	O	X	X	X	X

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x

PCH SM Bus address

Device	Address
DDR_IDIMM1	1010 000x A0h
GPU	1000 001x A0h
RTS455	1010 1100 A0h
RTD2166	1100 100 A0h
APS	1111 0100 A0h

SMBUS Control Table

	SOURCE	GPU	BATT	NECP388	SODIMM	SOC
SMB_EC_CK1	EC KB9022	X	V	X	X	X
SMB_EC_DA1	+3VALW		+3VALW			
SMB_EC_CK2	EC KB9022	V	X	X	X	V
SMB_EC_DA2	+3VS	+3VGS				+3VALW
PCH_SMBCLK	PCH	X	X	X	V	X
PCH_SMBDATA	+3VALW				+3VS	
PCH_SML0CLK	PCH	X	X	X	X	X
PCH_SML0DATA	+3VALW					
SML1CLK	PCH	V	X	V	X	X
SML1DATA	+3VALW	+3VGS		+3VS		

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V (RAM)	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Table

Item	BOM Structure
SKL only	SKL@
For 2+2	U22@
For 2+3	U23@
For 4+2	U42@
For DIS	DIS@
For UMA	UMA@
Camera	CMOS@
EMI pop	EMI@
EMI Un-pop	@EMI@
ESD pop	ESD@
ESD Un-pop	@ESD@
RF pop	RF@
RF unpop	@RF@
For SPI 8M	8M@
For SPI 16M	16M@
Finger Print	FP@
Keyboard backlight	KBL@
AOU	AOU@
NONAOU	NONAOU@
TYPEC FULL	TYPEC@
NONTYPEC	NONTYPEC@
APS	APS@
NOAPS	NOAPS@
2nd Battery USB	BATT2@
NO 2nd Battery USB	NOBATT2@
Onboard RAM HYNIX	X76DDR@
Onboard RAM MICRON	X76DDR@
Onboard RAM SAMSUNG	X76DDR@
VRAM HYNIX	X76H2G@
VRAM MICRON	X76M4G@
VRAM SAMSUNG	X76S2G@
CardReader RTS5146	X76RT@
CardReader GL835	X76GL@
TPM	TPM@
TCM	TCM@
NO TPM/TCM	NOTPM@
Connector	ME@

USB 2.0 Port Table

Port	3 External USB Port
1	USB 3.0 Port (AOU)
2	USB 3.0 Port
3	TYPE-C USB 3.0 Port
4	TYPE-C USB 3.0 Port(FULL)
5	Camera
6	M.2 BT
7	Card Reader
8	Finger Print
9	2nd Battery
10	

USB 3.0 Port Table

Port	USB 3.0 Port Table
1	USB 3.0 Port (AOU)
2	USB 3.0 Port
3	TYPE-C USB 3.0 Port
4	TYPE-C USB 3.0 Port(FULL)
5	
6	

SATA Port Table

Port	SATA Port Table
0	HDD
1	
2	M.2 SATA SSD

PCIe Port Table

Port	Lane	
1	1	GPU
2	2	
3	3	
4	4	
5		LAN
6		M.2 WLAN+BT
7		
8		
9		
10		M.2 PCIe*4 SSD
11		
12		

CPU

2+2

2+3

SKL-U

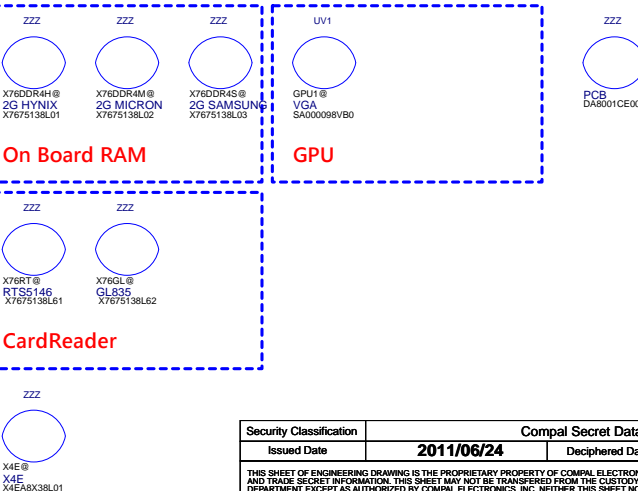
UC1 CPU1@ I7-6500U SA000092P60	UC1 CPU2@ I5-6300U SA000092T40	UC1 CPU3@ I5-6200U SA000092O70
UC1 CPU4@ I3-6005U SA0000ACN10	UC1 CPU10@ I5-7300U SA0000AD020	UC1 CPU11@ I5-7300U SA0000ADL30
UC1 CPU5@ I7-6500U SA00009E620	UC1 CPU6@ I5-6207U SA00009E530	UC1 CPU13@ I7-7567U SA0000AW620

KBL-U

UC1 CPU7@ I3-7100U SA0000A38H0	UC1 CPU8@ I5-7200U SA0000A37B0	UC1 CPU9@ I7-7500U SA0000A34F0
UC1 CPU10@ I5-7300U SA0000AD020	UC1 CPU11@ I5-7300U SA0000ADL30	UC1 CPU12@ I445U SA0000ADV40
UC1 CPU13@ I7-7567U SA0000AW620	UC1 CPU14@ I5-7267U SA0000AKR20	

KBL-RU 4+2

UC1 CPU15@ KBL-R QN5D SA0000AR010	UC1 CPU16@ KBL-R QN5C SA0000AQZ10
UC1 CPU17@ KBL-R QNEF SA0000AWB00	UC1 CPU18@ KBL-R QNBF SA0000AWC00



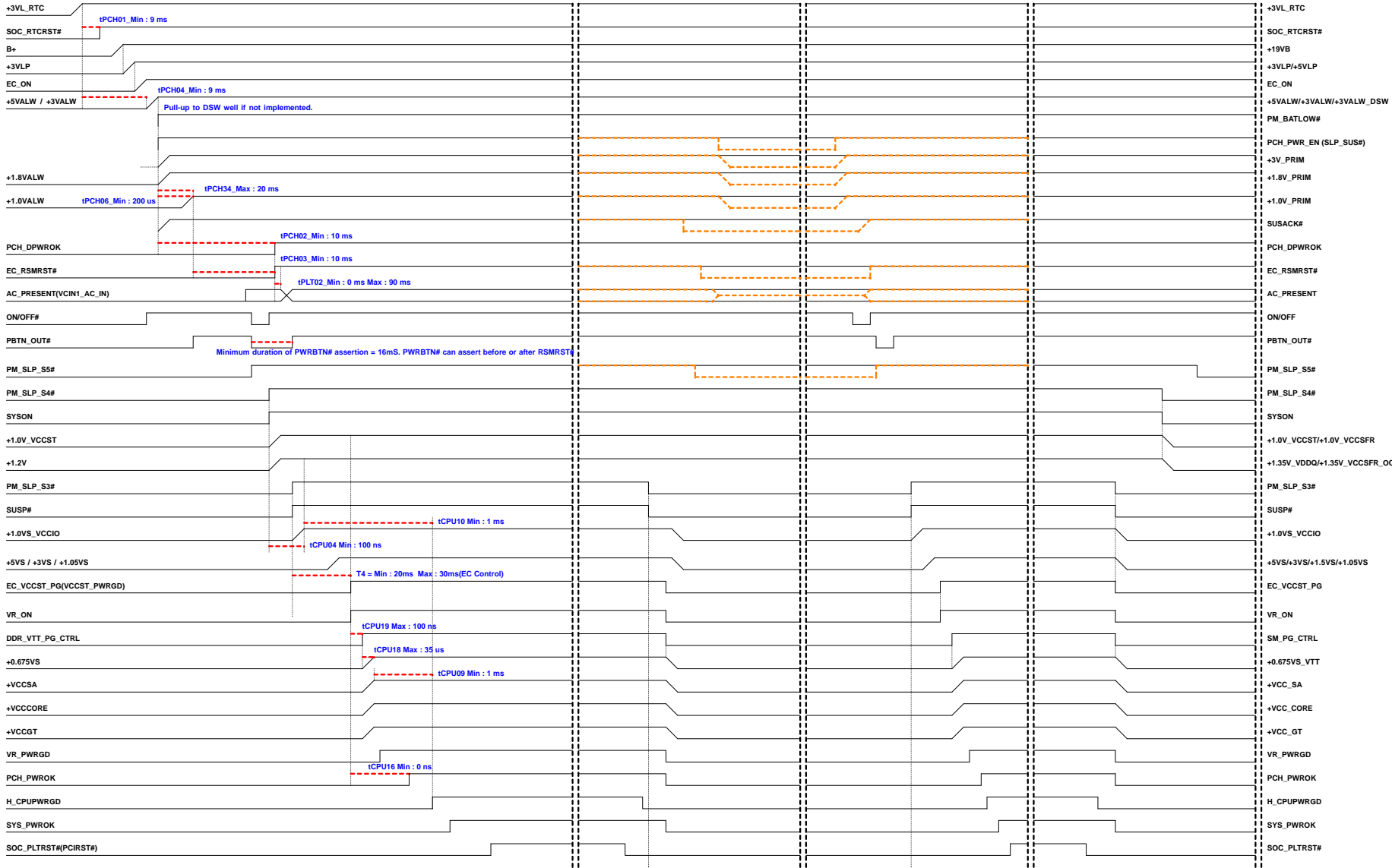
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		Size	Document Number
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G3->S0

S0->S3/DS3

S3/DS3->S0

S0->S5



M1-30 VRAM STRAP

X76@		X76@					
	Vendor uv3, uv4, uv5, uv6	ID	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV22	R_pd RV27
X76H2G@ X7667538L03	HYNIX 4096Mbits 2GBytes SA000076P80 TEMP 256MX16 K4W4G1646E-BC1A TEMP	0	0	0	0	NC	4.75K
X76M2G@ X7667538L04	Micron 4096Mbits 2GBytes SA00009HF00 TEMP 256Mx16 MT41J256M16LY-091G:N	TEMP1	0	0	1	8.45K	2K
X76S2G@ X7667538L05	SAMSUNG 4096Mbits 2GBytes SA00008DN00 TEMP 256MX16 H5TC4G63CFR-N0C TEMP	2	0	1	0	4.53K	2K
		4	1	0	0	4.53K	4.99K
		5	1	0	1	3.24K	5.62K
		6	1	1	0	3.4K	10K

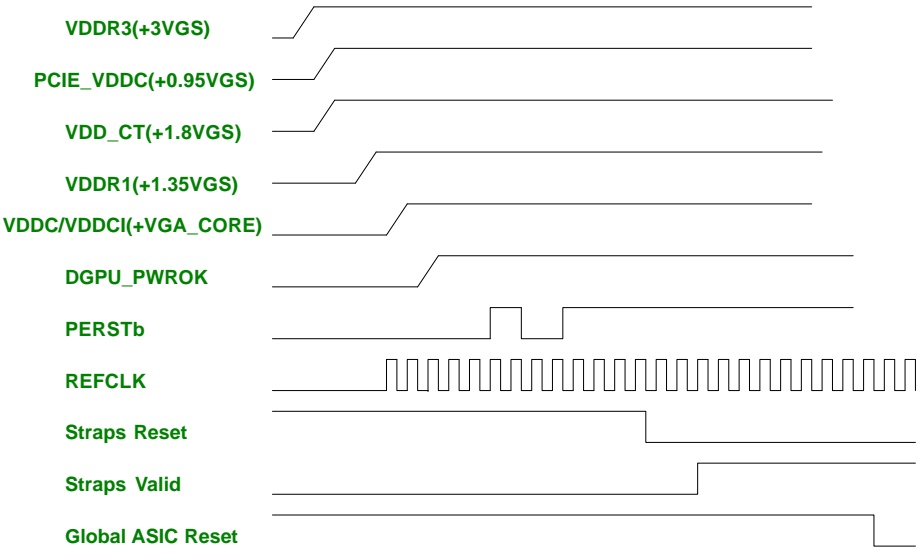


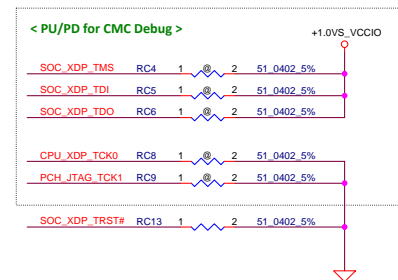
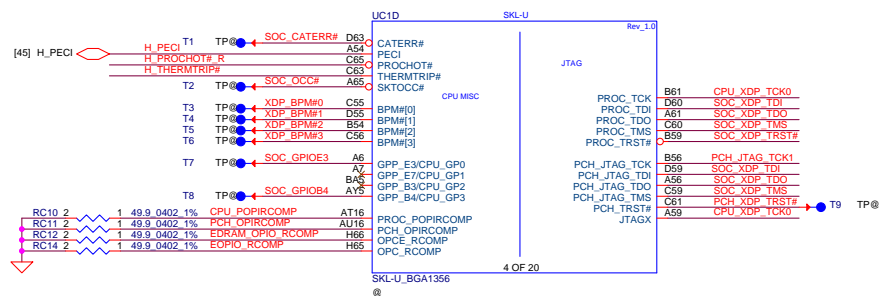
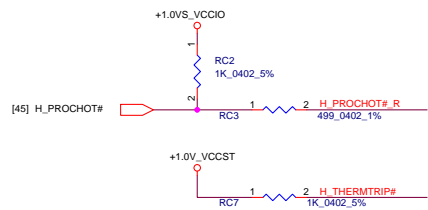
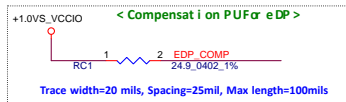
R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111
Note: 0402 1% resistors are required.		

Power-Up/Down Sequence

"M1" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

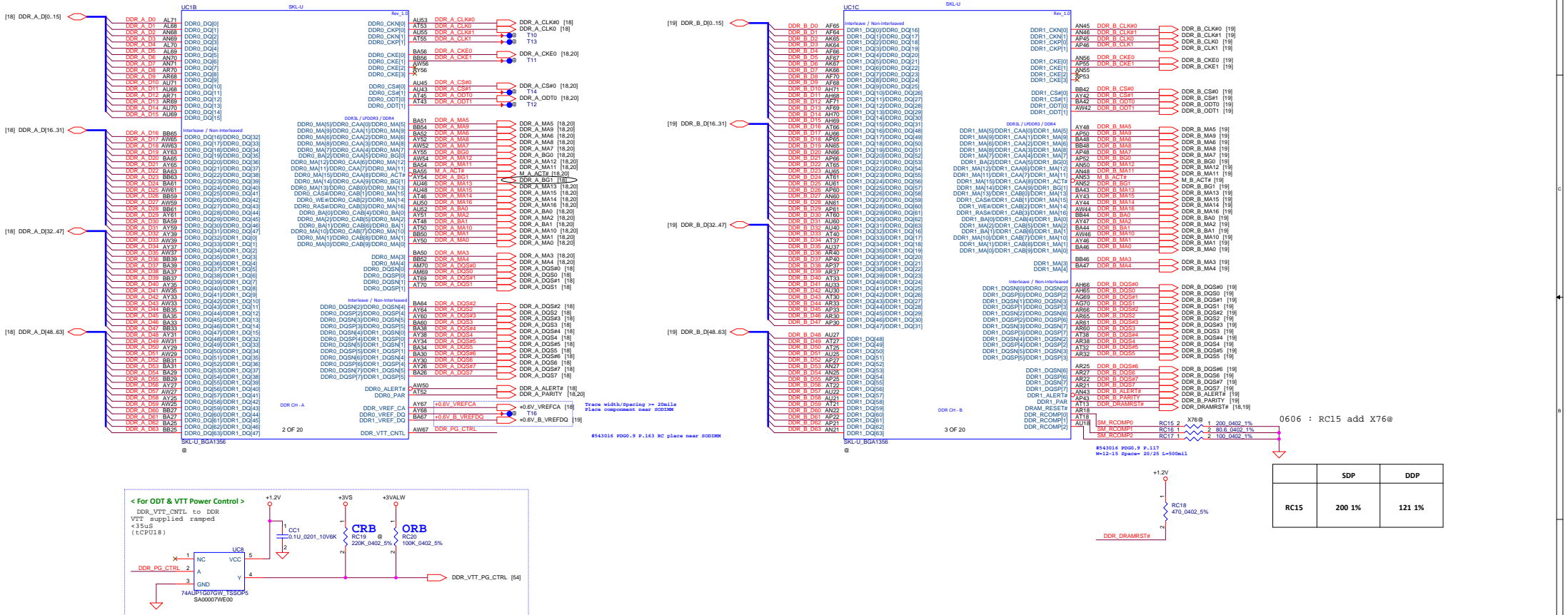
- All the ASIC supplies must reach their respective nominal voltages within 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
- The maximum slew rate on all rails is 50 mV/μs.
- It is recommended that the 3.3-V rail ramp up first.
- It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2ms from the start of VDDC ramping up.
- The power rails that are shared with other components on the system should be gated for the dGPU so that when dGPU is powered down (for example AMD PowerXpress™ idle state), all the power rails are removed from the dGPU.
- The gate circuits must meet the slew rate requirement (such as $\leq 50\text{mV/us}$)
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



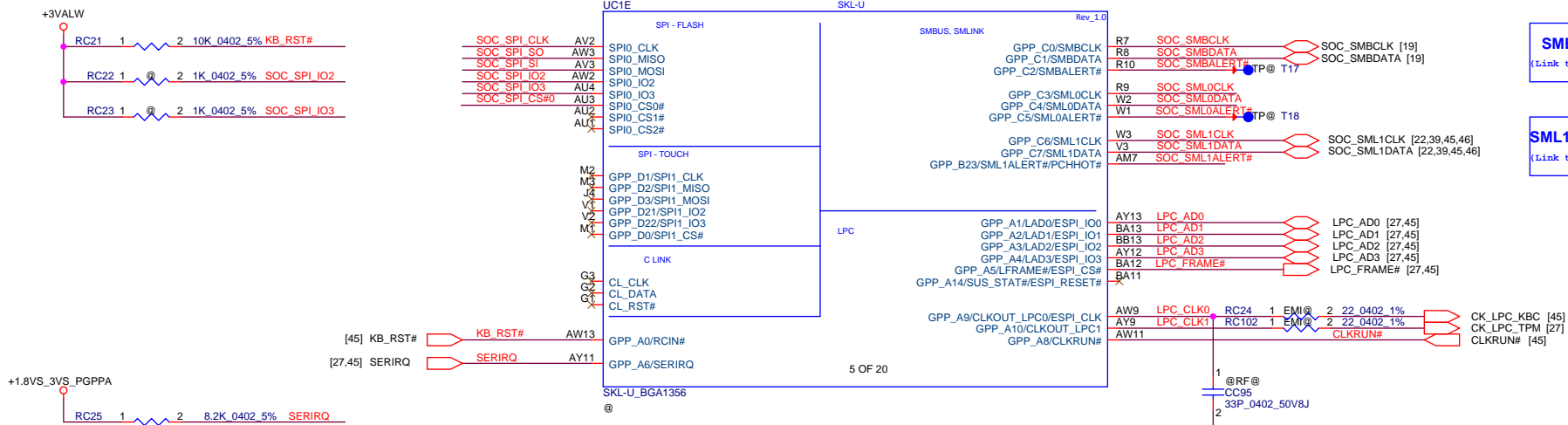


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Interleaved Memory



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Customer				LA-D562P	
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SMBALERT# (Internal Pull Down):

0 = Disable Intel ME TLS function ==> Default

1 = Enable Intel ME TLS function

SML0ALERT# (Internal Pull Down):

eSPI or LPC

0 = LPC is selected for EC ==> Default

1 = eSPI is selected for EC

SMB
(Link to DDR)

SML1
(Link to EC,DGPU,CRT,APS,RT85455)

[45] KB_RST#
[27,45] SERIRQ

< SPI ROM - 8M >

UC9 8M@
1 /CS VCC
2 /DO(IO1) /HOLD(IO3)
3 /WP(IO2) CLK
4 GND DI(IO0)

UC9
16M@
16M ROM
SA00005VV20

SOC_SML1ALERT# RC26 2 150K 0402_5%
SOC_SML0CLK RC27 1 499 0402_1%
SOC_SML0DATA RC28 1 499 0402_1%
SOC_SMBCLK 1 8
SOC_SMBDATA 2 7
SOC_SML1DATA 3 6
SOC_SML1CLK 4 5
1K_0804_8P4R_5%

CLKRUN# RC30 1 8.2K 0402_5%
Follow 543016_SKL_U_Y_PDG_0_9

RPC1, RPC3 and RC30 are close to UC3

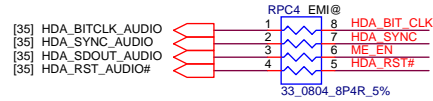
From CPU
SOC_SPI_I02 1 8 SOC_SPI_I02_0 R
SOC_SPI_SO 2 7 SOC_SPI_SO_0 R
SOC_SPI_SI 3 6 SOC_SPI_SI_0 R
SOC_SPI_I03 4 5 SOC_SPI_I03_0 K
SOC_SPI_CLK 1 2 SOC_SPI_CLK_0 R
33_0804_8P4R_5%
RC29 1 2 33_0402_5%

From EC
[45] EC_SPI_CS# SOC_SPI_CS# 1 8
[45] EC_SPI_MOSI EC_SPI_MOSI 2 7
[45] EC_SPI_CLK EC_SPI_CLK 3 6
[45] EC_SPI_MISO EC_SPI_MISO 4 5

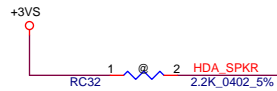
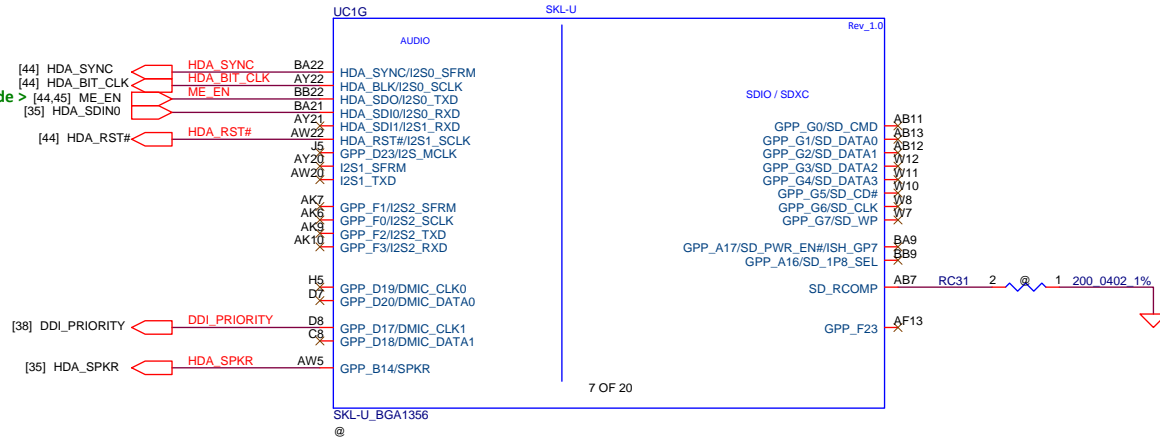
For ENE auto load search code V12
+3VALW
RC110 1 10K 0402_5%
SOC_SPI_CS# 2

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< HD AUDIO >



< To Enable ME Override >

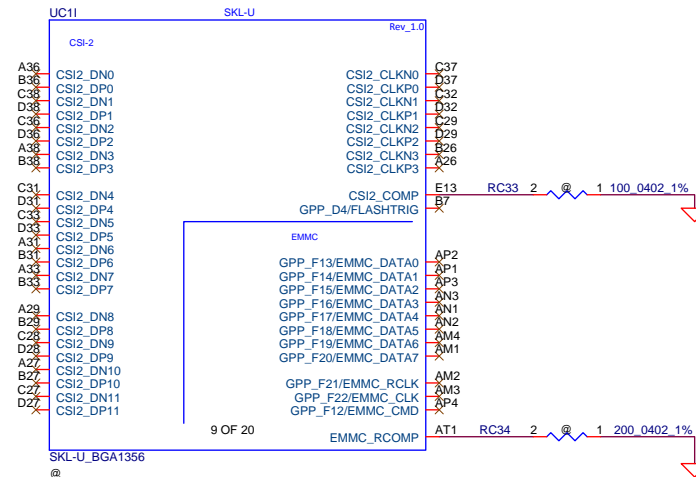


SPKR (Internal Pull Down):

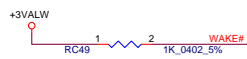
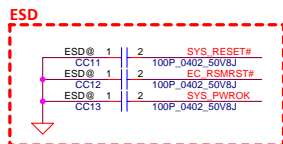
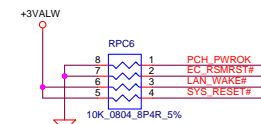
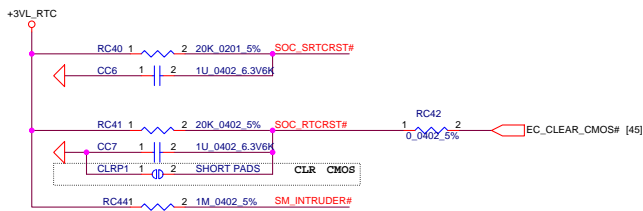
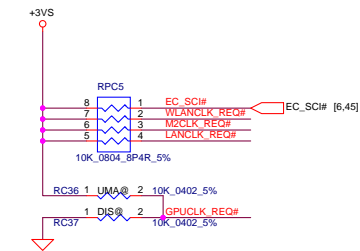
TOP Swap Override

0 = Disable TOP Swap mode. ==> Default

1 = Enable TOP Swap Mode.



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From EC (Open-Drain)

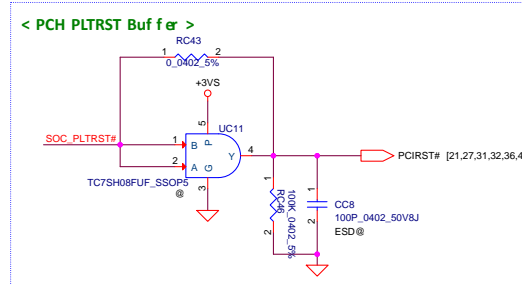
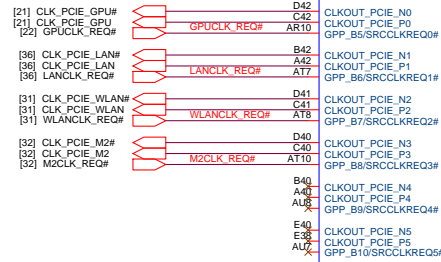


DGPU

LAN

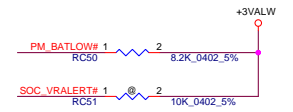
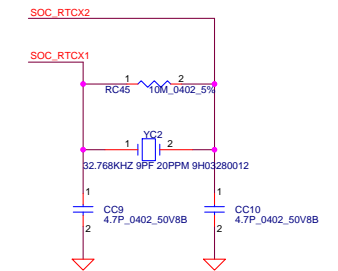
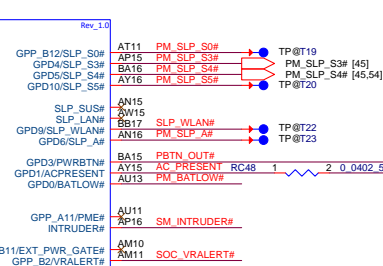
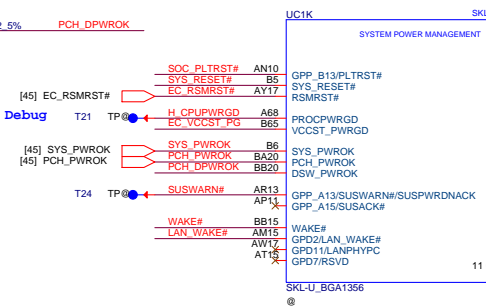
NGFF WL+BT(KEY E)

M.2 PCIE SSD



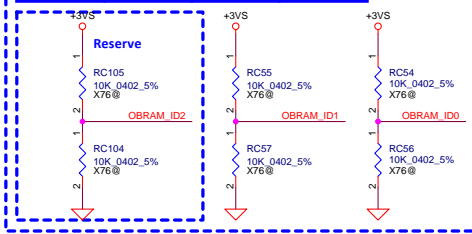
EC_RSMRST# RC47 1 2 0.0402_5% PCH_DPWRK

Only For Power Sequence Debug



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RAM vender	OBRAM_ID2	OBRAM_ID1	OBRAM_ID0
Hynix	1	1	1
Micron	1	1	0
Samsung	1	0	1
	1	0	0



GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

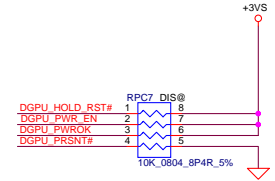
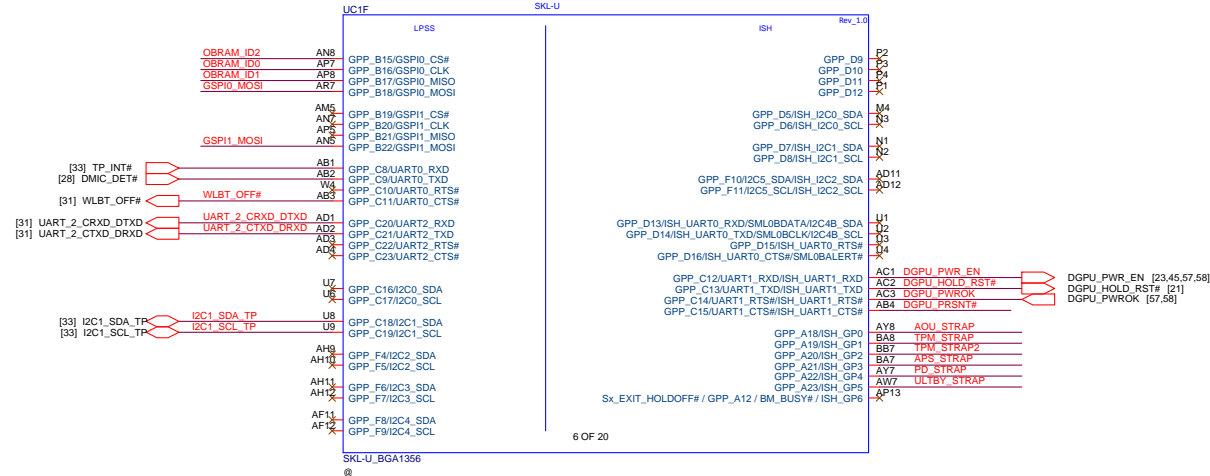
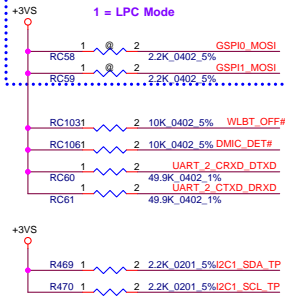
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1_MOSI (Internal Pull Down):

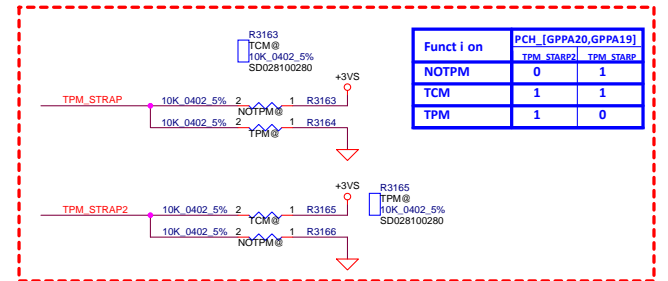
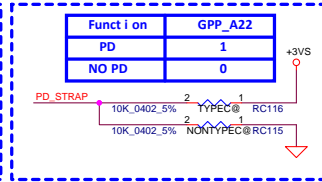
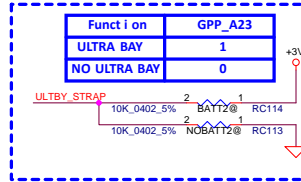
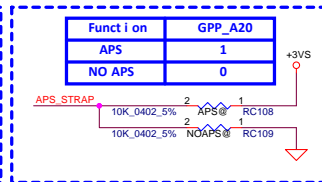
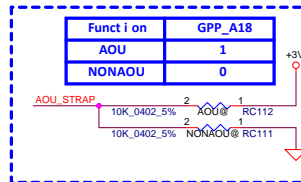
Boot BIOS Strap Bit

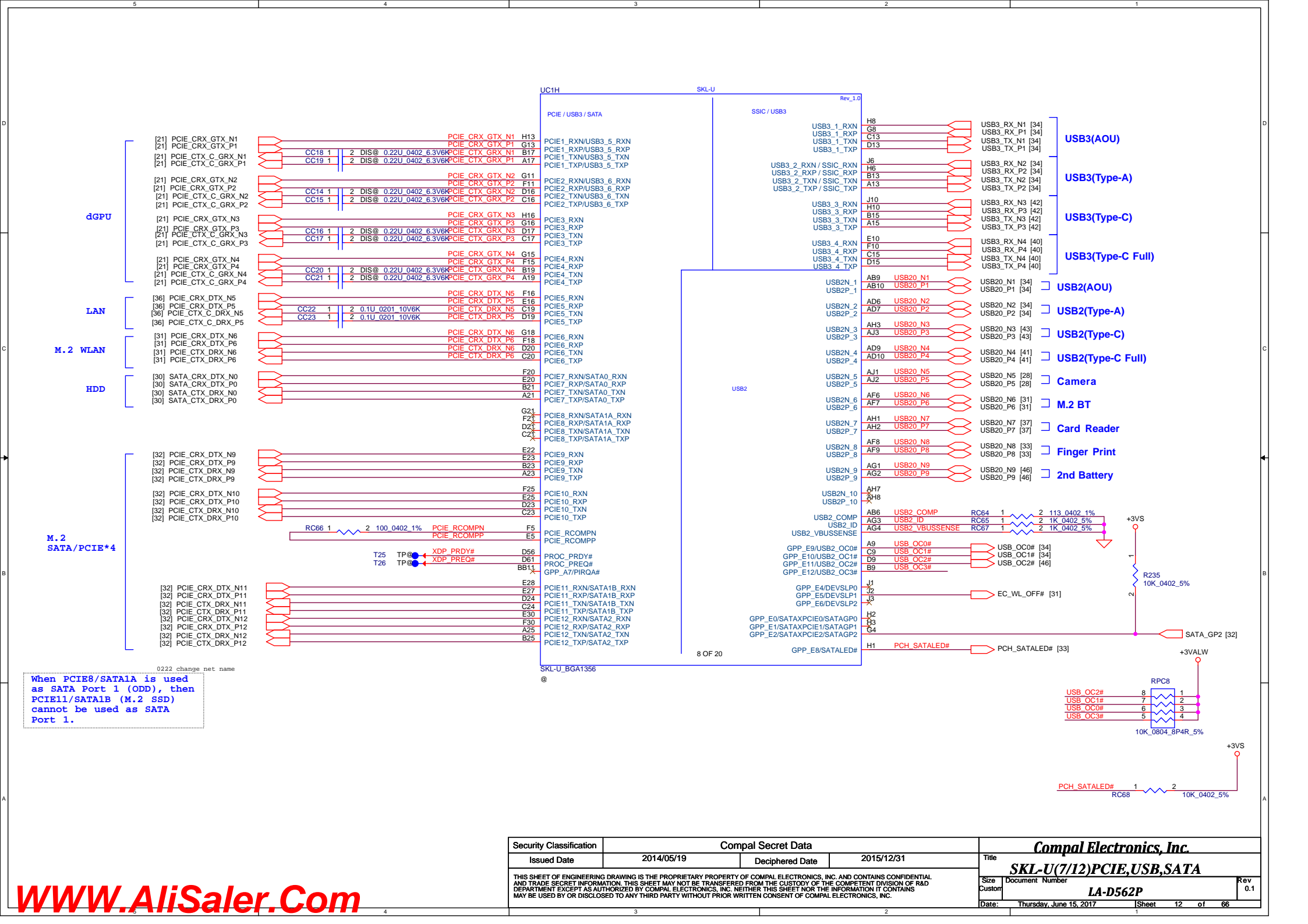
0 = SPI Mode ==> Default

1 = LPC Mode



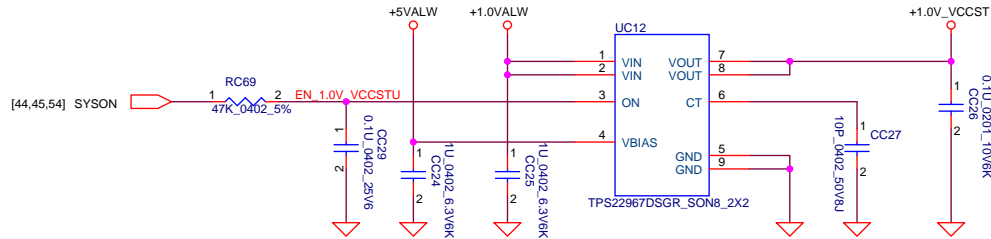
Function	GPP_C15
UMA	1
DIS	0





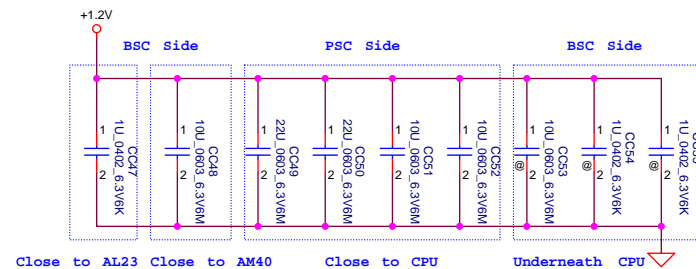
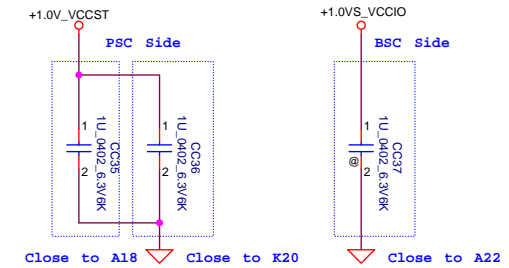
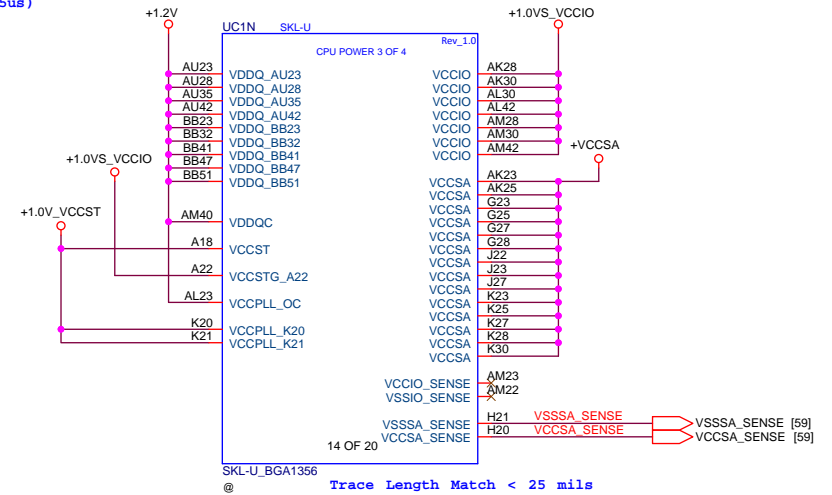
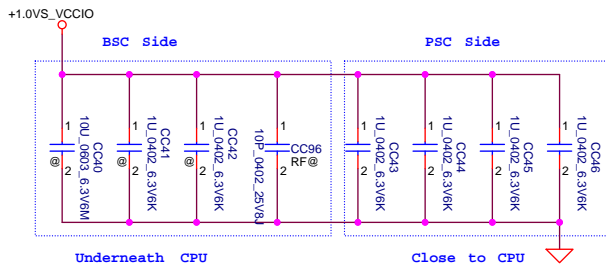
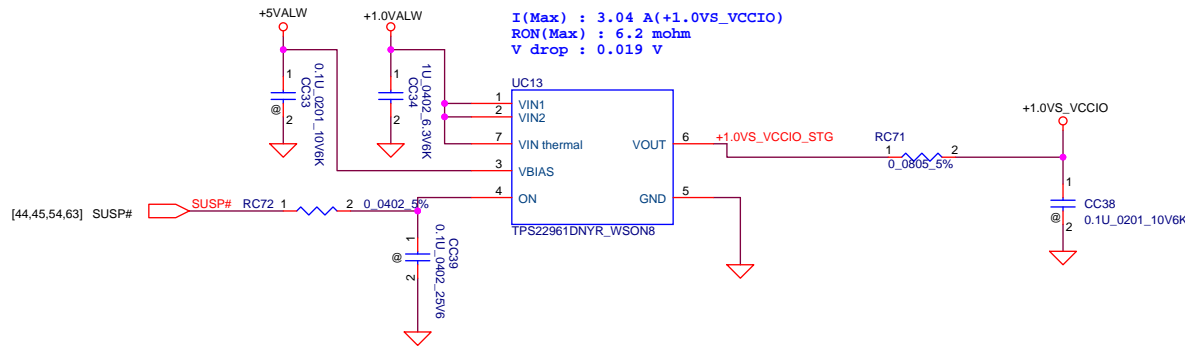
+1.0VALW TO +1.0V_VCCST

I(Max) : 0.16 A(+1.0V_VCCST)
RON(Max) : 25 mohm
V drop : 0.004 V

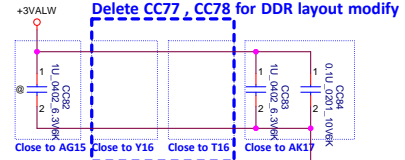
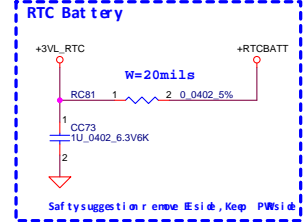
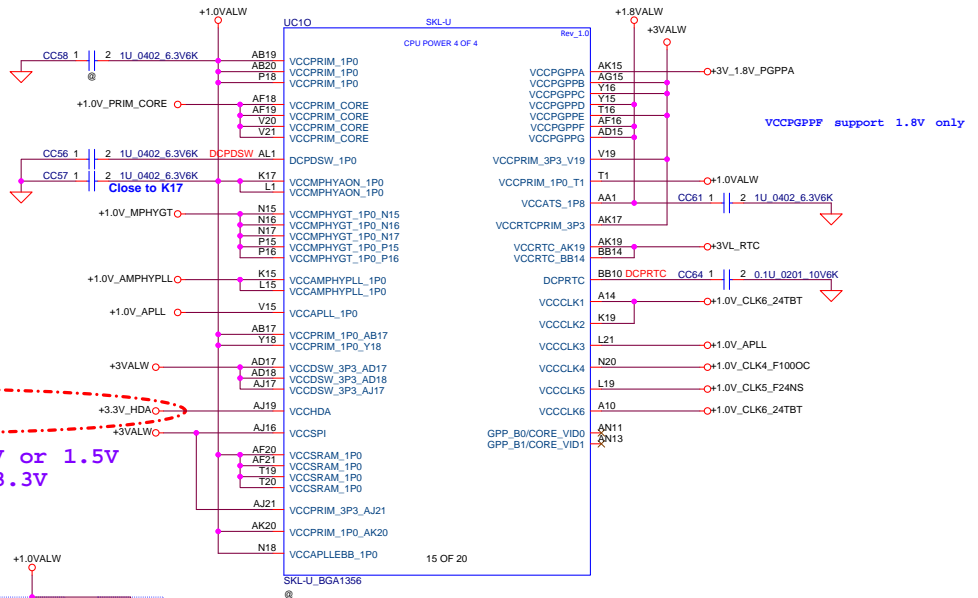
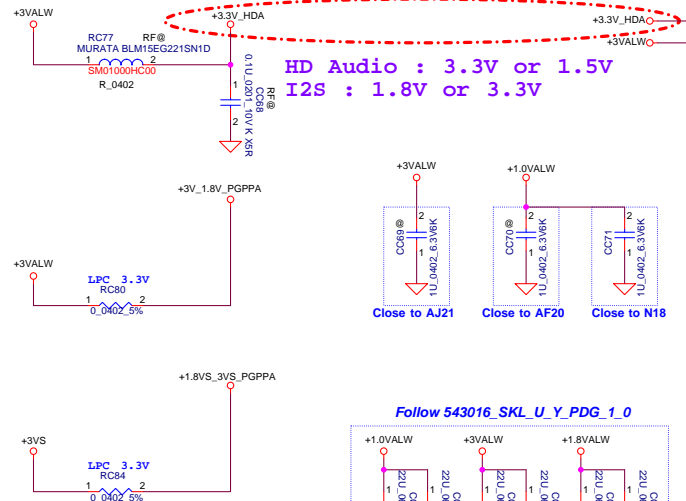
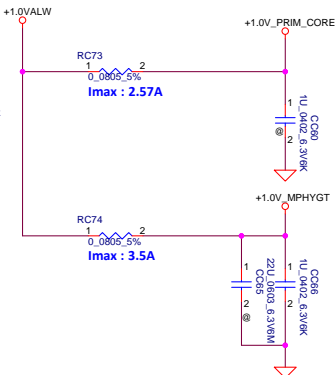
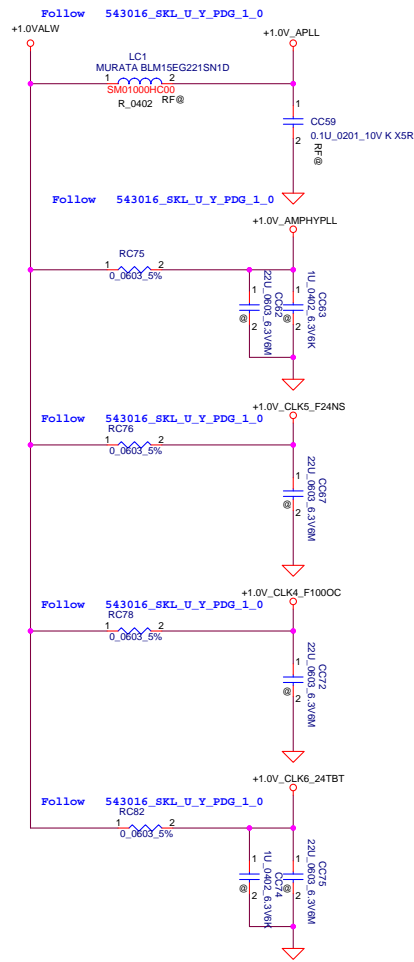


+1.0VALW TO +1.0VS_VCCIO

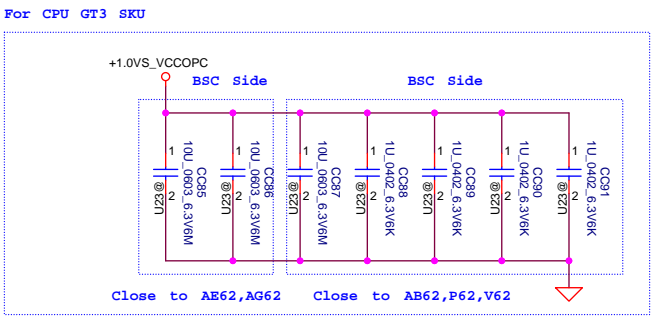
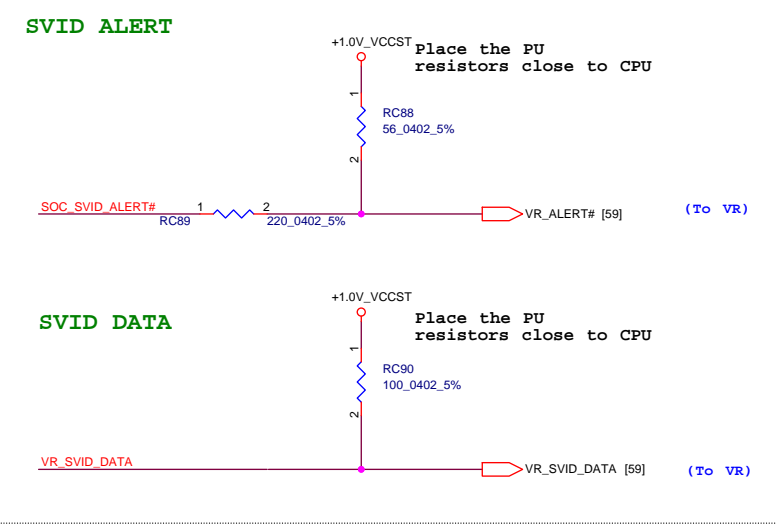
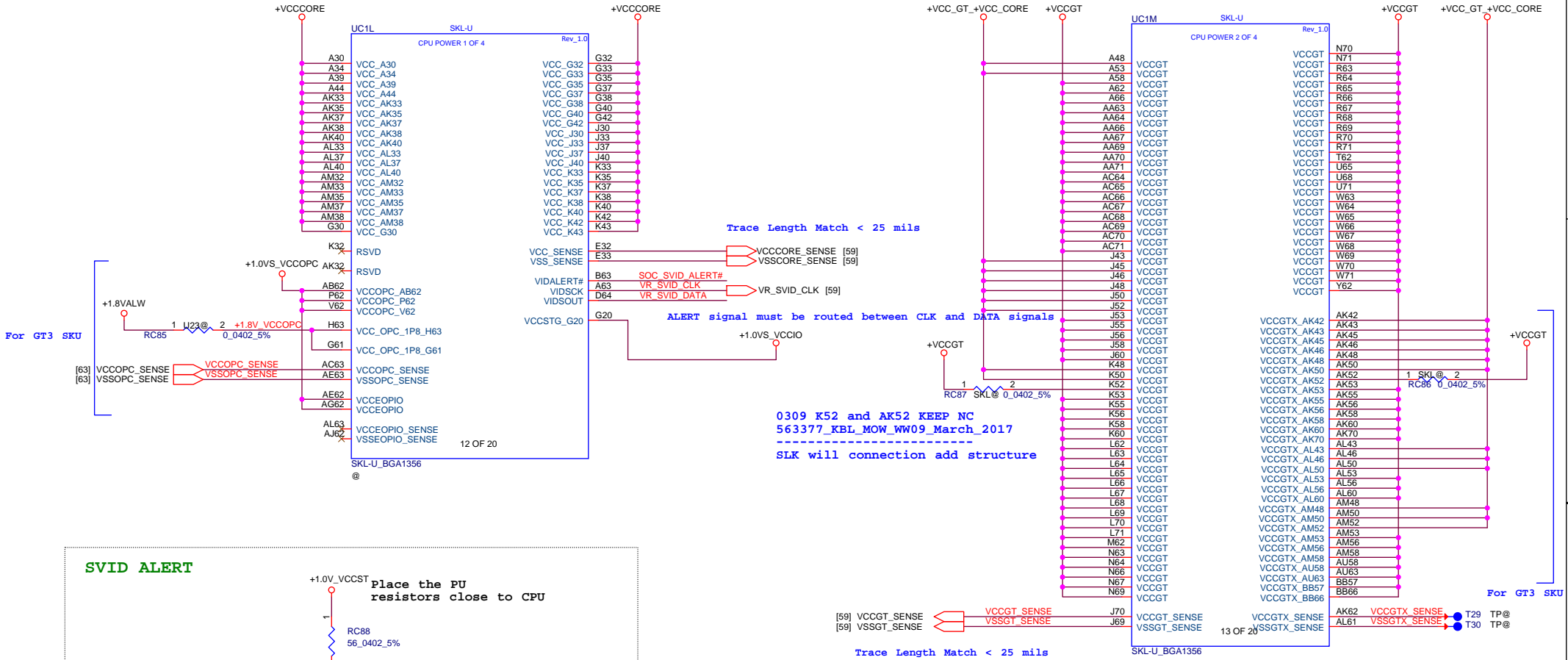
I(Max) : 3.04 A(+1.0VS_VCCIO)
RON(Max) : 6.2 mohm
V drop : 0.019 V



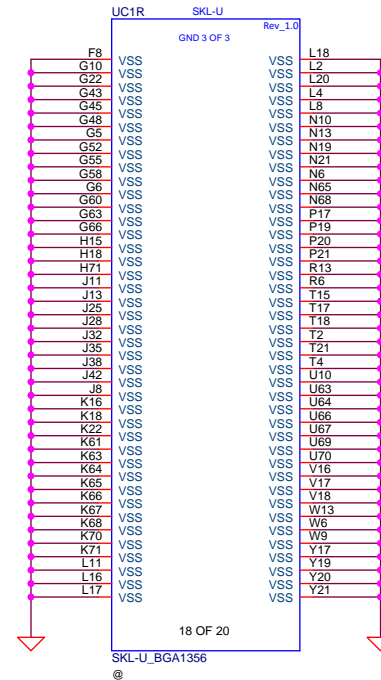
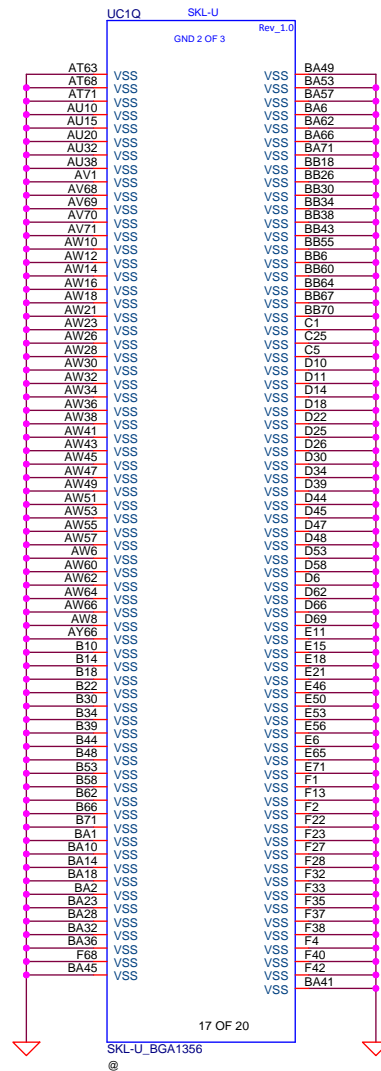
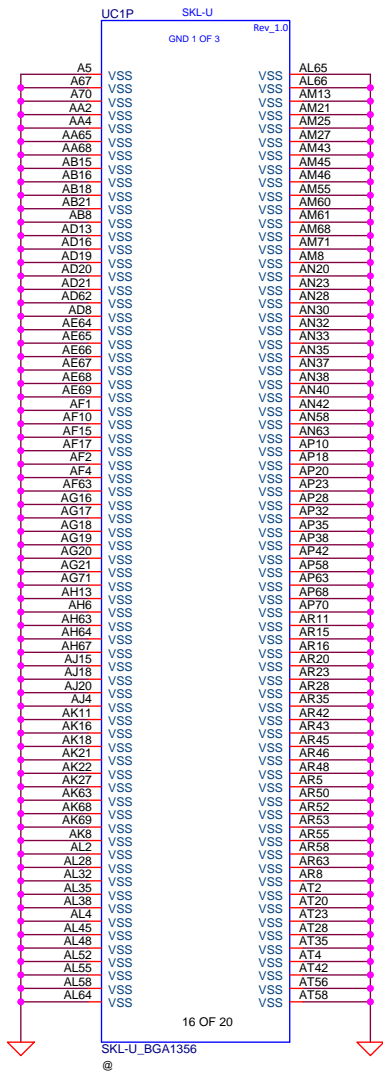
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/05/19	Deciphered Date	2015/12/31	Title	
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Size	Custom	Document Number	LA-D562P	Rev	0.1
Date:	Thursday, June 15, 2017	Sheet	13	of	66



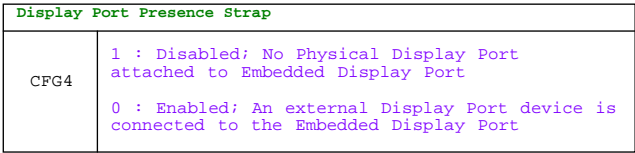
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Issued Date	2014/05/19	Deciphered Date	2015/12/31	Title	SKL-U(9/12)Power
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				Custom	LA-D562P
				Date:	Thursday, June 15, 2017
				Sheet	14 of 66



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Issued Date	2014/05/19	Deciphered Date	2015/12/31	Size		LA-D562P	
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				Date:	Thursday, June 15, 2017	Sheet	15 of 66



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Size		Document Number		Rev	
Custom		LA-D562P		0.1	
Date:		Thursday, June 15, 2017		Sheet	16 of 66

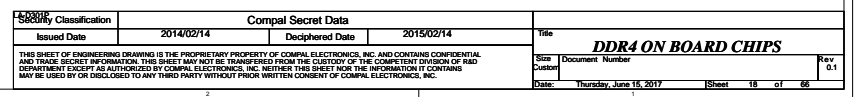


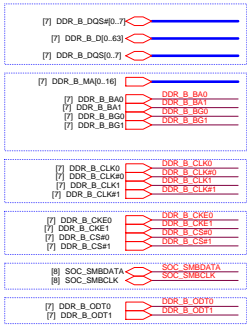
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Issued Date	2014/05/19	Deciphered Date	2015/12/31	Title	
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[7] DDR_A_BG1 

LOGIC

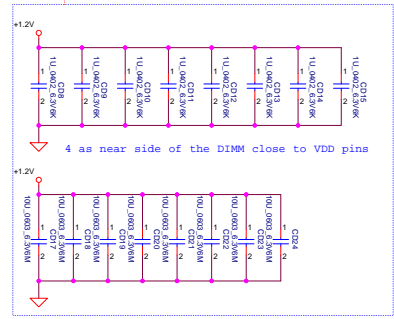
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DQL0	D3	DQL0	D19	DQL0	D35	DQL0	D51
DQL1	D1	DQL1	D17	DQL1	D33	DQL1	D49
DQL2	D2	DQL2	D18	DQL2	D34	DQL2	D50
DQL3	D0	DQL3	D16	DQL3	D32	DQL3	D48
DQL4	D7	DQL4	D23	DQL4	D39	DQL4	D55
DQL5	D5	DQL5	D21	DQL5	D37	DQL5	D53
DQL6	D6	DQL6	D22	DQL6	D38	DQL6	D54
DQL7	D4	DQL7	D20	DQL7	D36	DQL7	D52
DQU0	D10	DQU0	D26	DQU0	D42	DQU0	D58
DQU1	D8	DQU1	D24	DQU1	D40	DQU1	D56
DQU2	D11	DQU2	D27	DQU2	D43	DQU2	D59
DQU3	D9	DQU3	D25	DQU3	D41	DQU3	D57
DQU4	D14	DQU4	D30	DQU4	D46	DQU4	D62
DQU5	D13	DQU5	D29	DQU5	D45	DQU5	D61
DQU6	D15	DQU6	D31	DQU6	D47	DQU6	D63
DQU7	D12	DQU7	D28	DQU7	D44	DQU7	D60



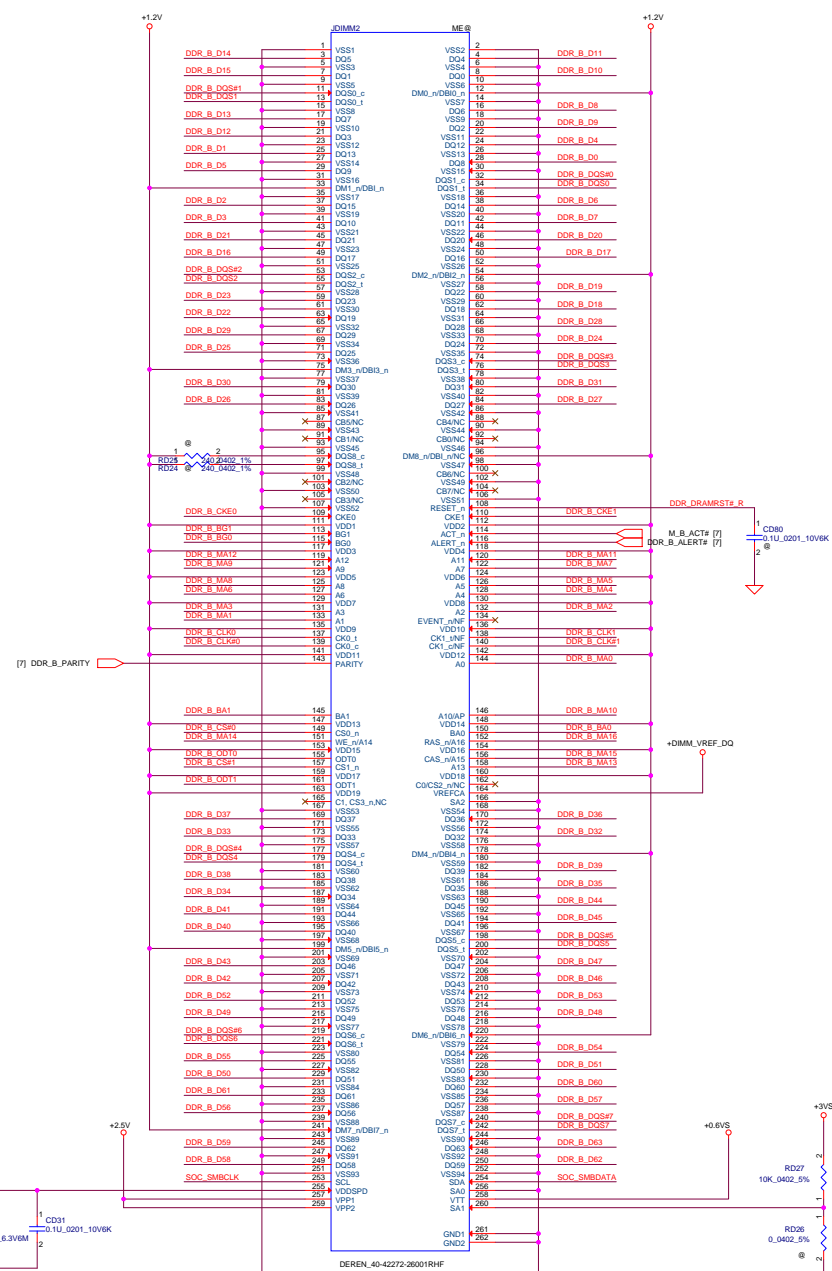
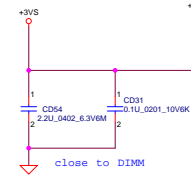
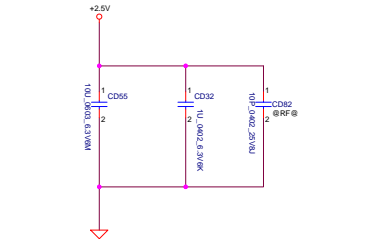
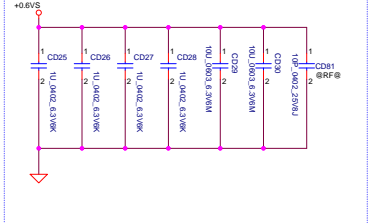


Layout Note: Place near JDIMM1

Note: Check voltage tolerance of VREF_DQ at the DIMM socket

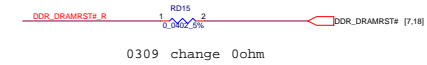
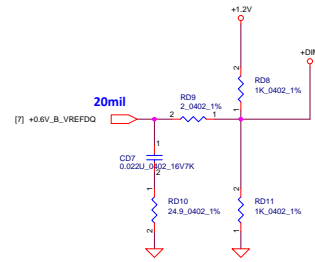


Place these caps on the VT plane close to DIMM



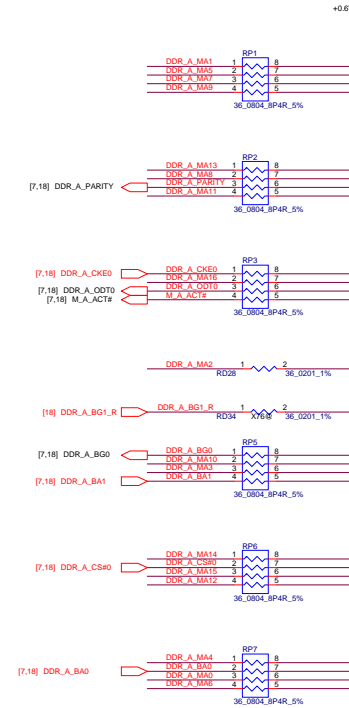
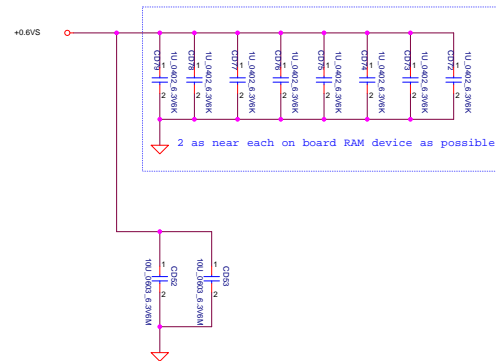
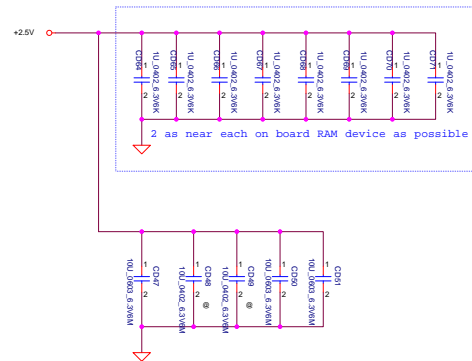
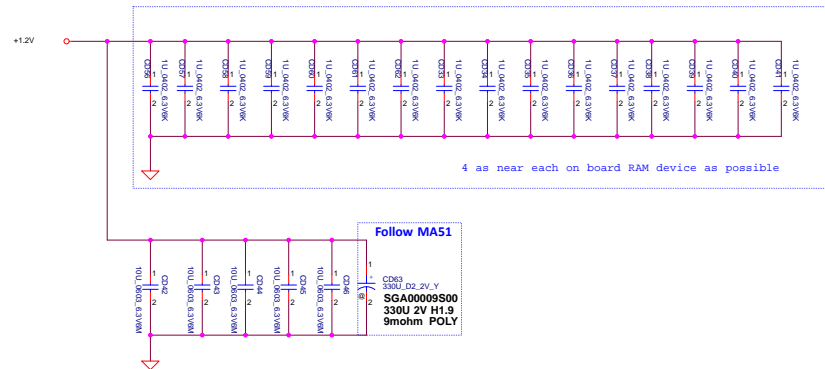
JDIMM Connector PN
SP07001GK00

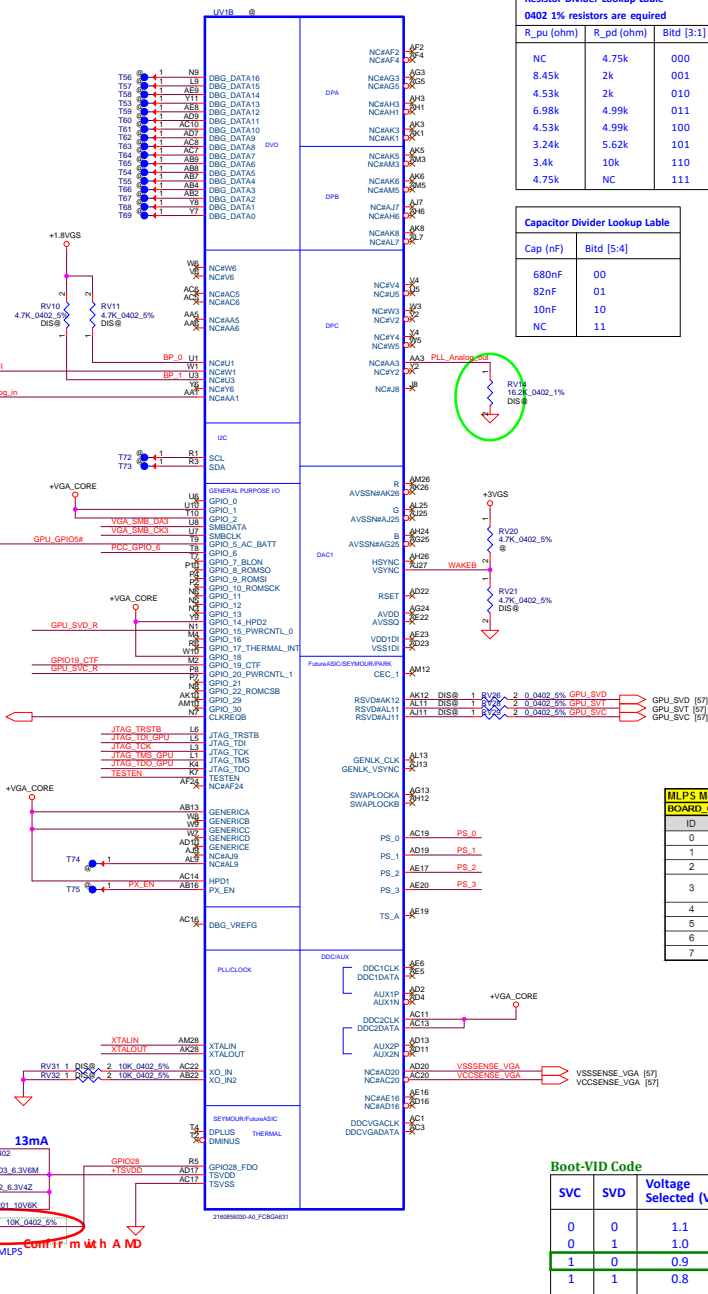
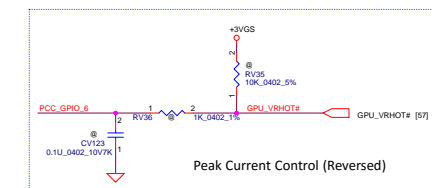
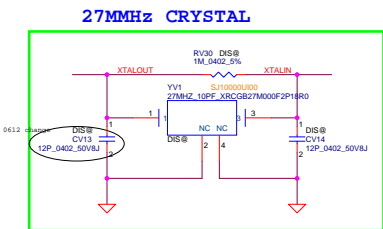
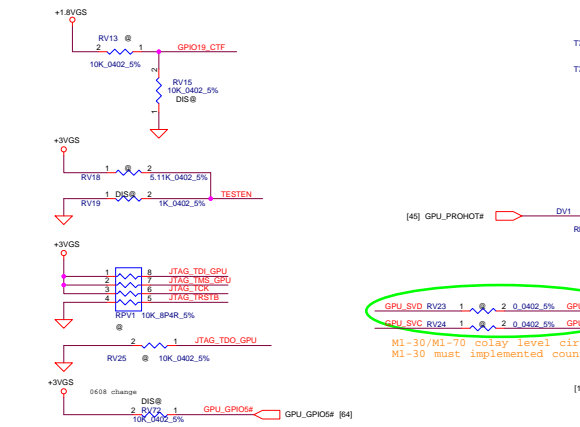
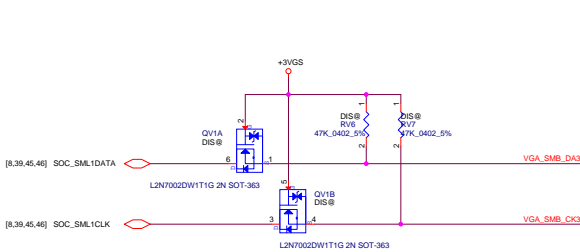
Reverse Type
2-3A to 1 DIMMs/channel



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				Date:	Thursday, June 15, 2017
				Sheet	19 of 66

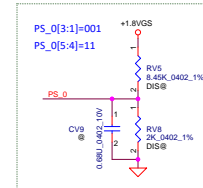
[7,18] DDR_A_MA[0..16] 



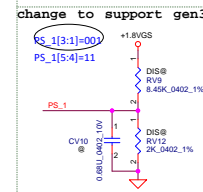


Resistor Divider Lookup Table			
0402 1% resistors are required			
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]	
NC	4.75k	000	
8.45k	2k	001	
4.53k	2k	010	
6.98k	4.99k	011	
4.53k	4.99k	100	
3.24k	5.62k	101	
3.4k	10k	110	
4.75k	NC	111	

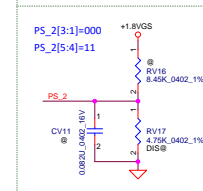
Capacitor Divider Lookup Table		
Cap (nF)	Bitd [5:4]	
680nF	00	
82nF	01	
10nF	10	
NC	11	



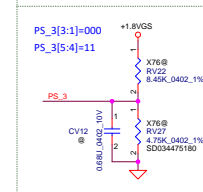
Strap Name :	
PS_0[3:1]=001	PS_0[1] ROM_CONFIG[0]
PS_0[5:4]=11	PS_0[2] ROM_CONFIG[1]
	PS_0[3] ROM_CONFIG[2]
	PS_0[4] N/A
	PS_0[5] AUD_PORT_CONN_PINSTRAP[0]



Strap Name :	
PS_1[3:1]=001	PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[5:4]=11	PS_1[2] TRAP_CLK_PM_EN
	PS_1[3] N/A
	PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
	PS_1[5] STRAP_TX_DEEMPH_EN



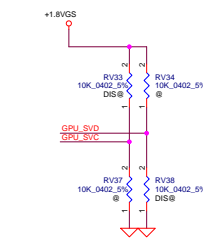
Strap Name :	
PS_2[3:1]=000	PS_2[1] N/A
PS_2[5:4]=11	PS_2[2] N/A
	PS_2[3] STRAP_BIOS_ROM_EN
	PS_2[4] STRAP_BIF_VGA_DIS
	PS_2[5] N/A



Strap Name :	
PS_3[3:1]=000	PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[5:4]=11	PS_3[2] BOARD_CONFIG[1] (Memory ID)
	PS_3[3] BOARD_CONFIG[2] (Memory ID)
	PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
	PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

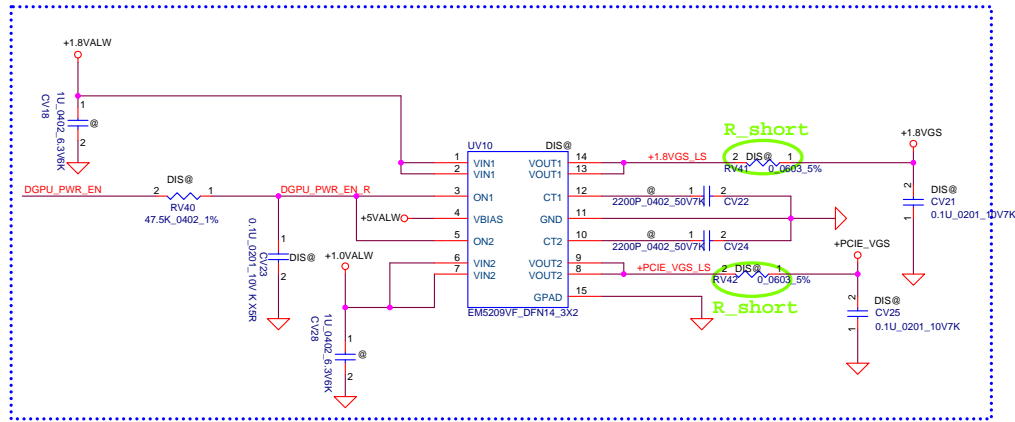
VRAM Type
Need reference
X76 Schematic

MLPS Memory ID setting							
BOARD_CONFIG[2:0]							
ID	[2:0]	Memory Type	Configuration	Row x Col x Bank bits	Channel Size	Vendor PIN	SMT quantity
0	000	ex: Samsung-GDDR6	64M x 32 4PCS		1GB	K4G80325FB-HC28	4 pcs
1	001	Samsung-GDDR6	256M*32 2PCS, 1 Rank		1GB	H50CBH424MUR-ROD	2 pcs
2	010	Hynix-GDDR6	256M*32 2PCS, 1 Rank		1GB	MT51J256M32HP-70-A	2 pcs
3	011						
4	100						
5	101						
6	110						
7	111						

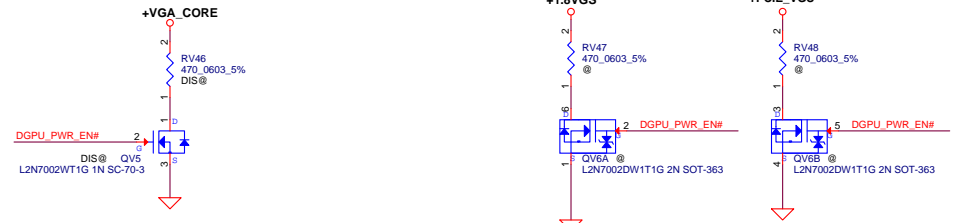
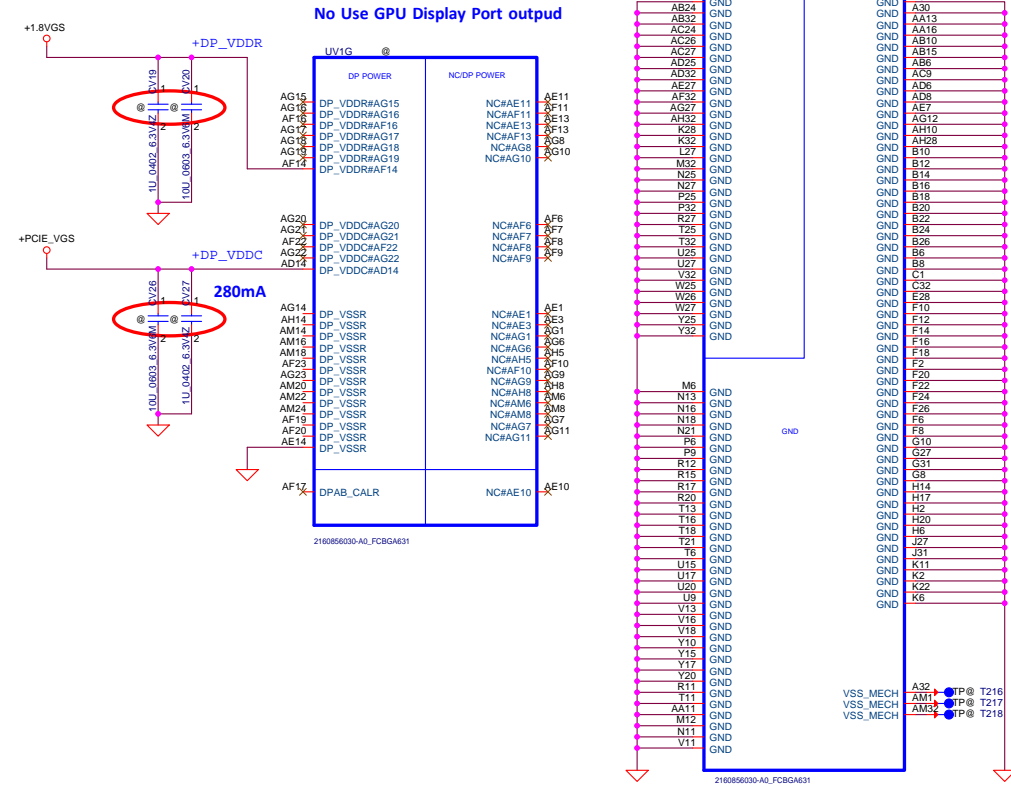
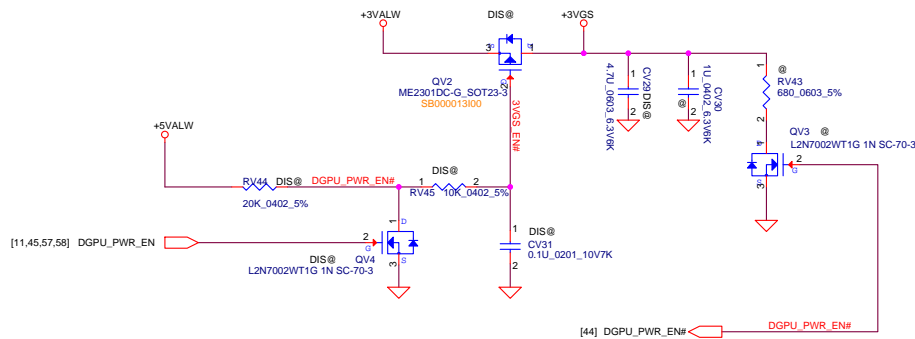


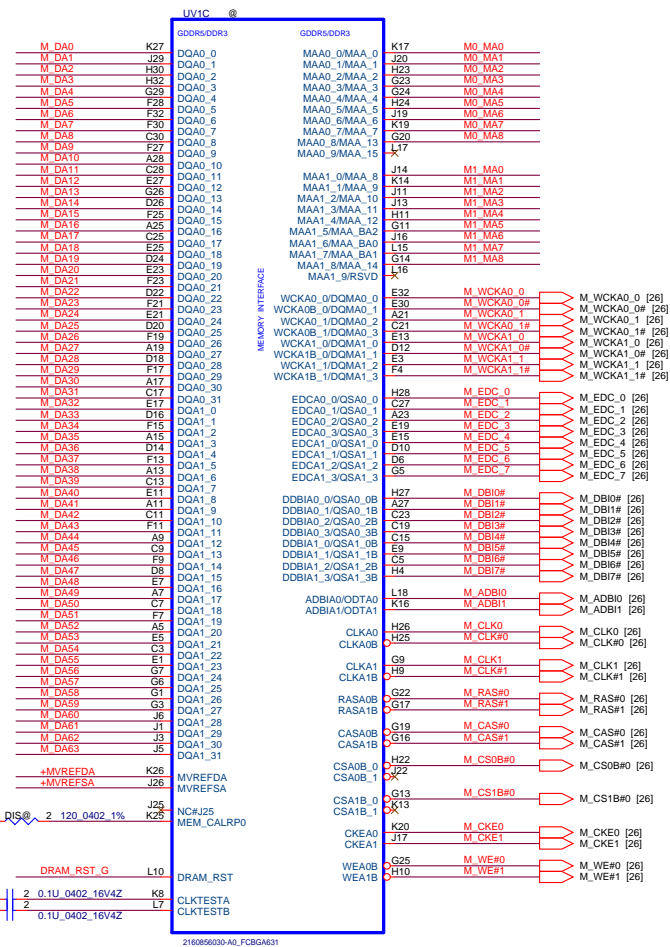
Boot-VID Code		
SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

+1.8VALW TO +1.8VGS **+1.0VALW TO +PCIE_VGS** **Load switch**



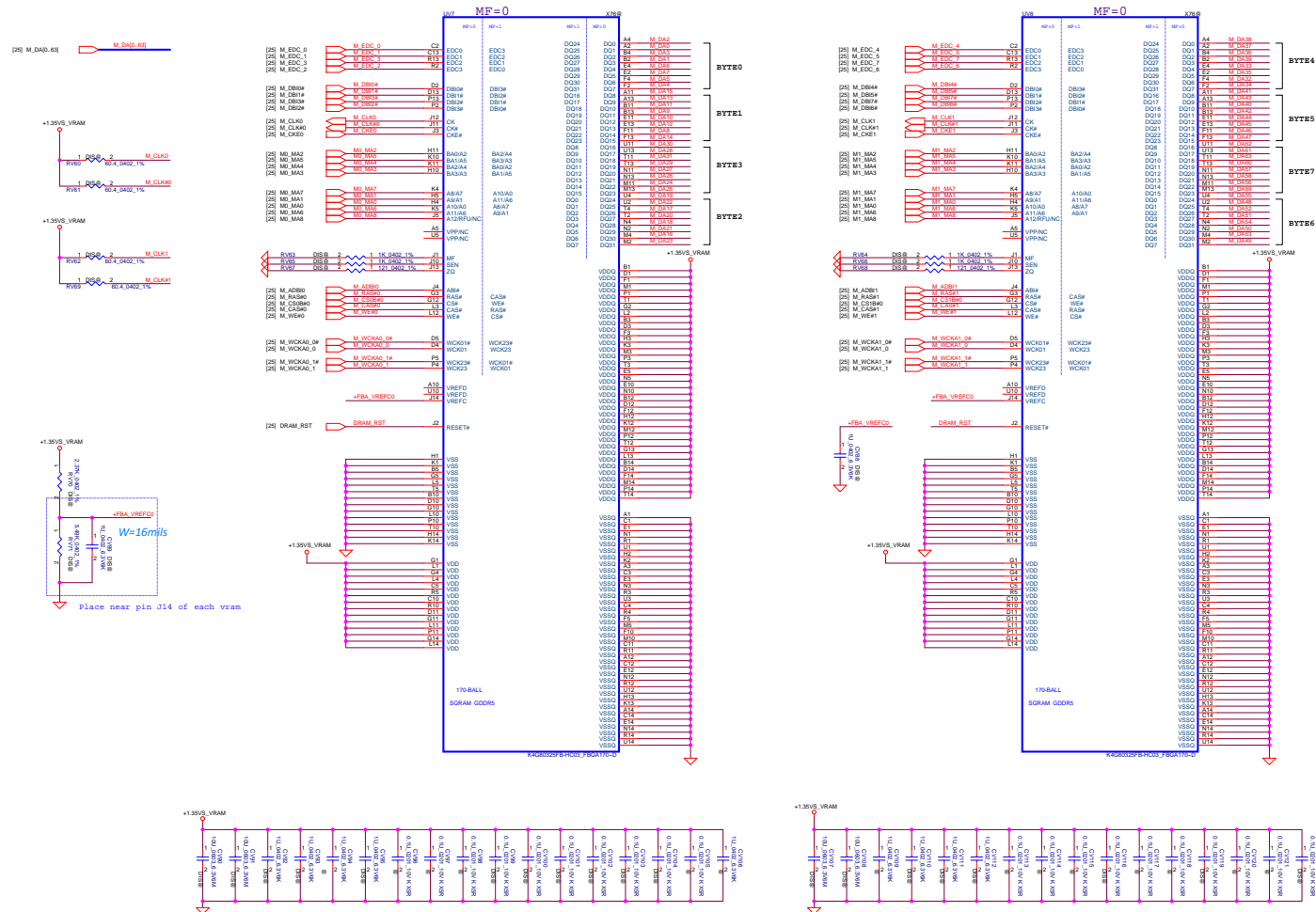
+3VALW to +3VGS





1 2 3 4 5 Date: Thursday, June 15, 2017 Sheet 25 of 66

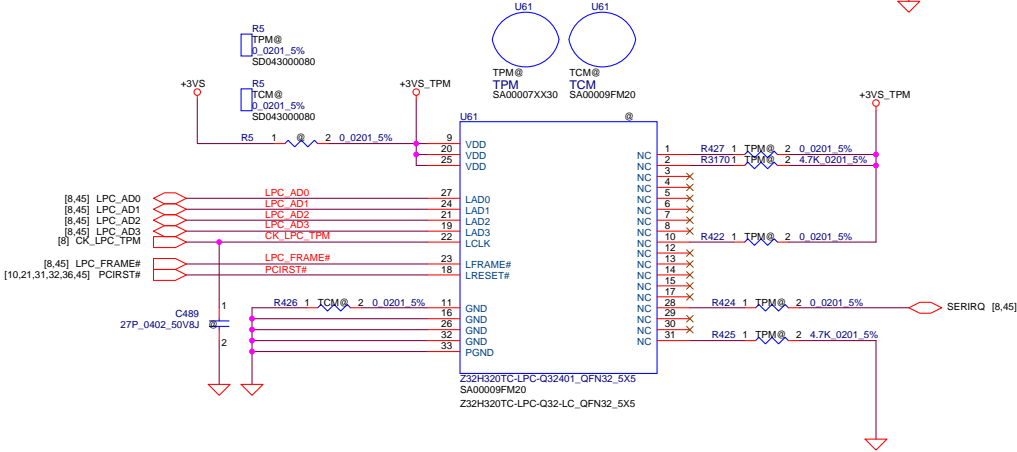
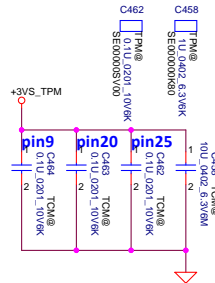
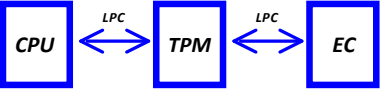
Memory Partition A



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Issued Date	2016/12/05	Deciphered Date	2017/12/05	Title GDDR5 A0
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			Date Thursday, June 15, 2017	
			Page 26 of 68	

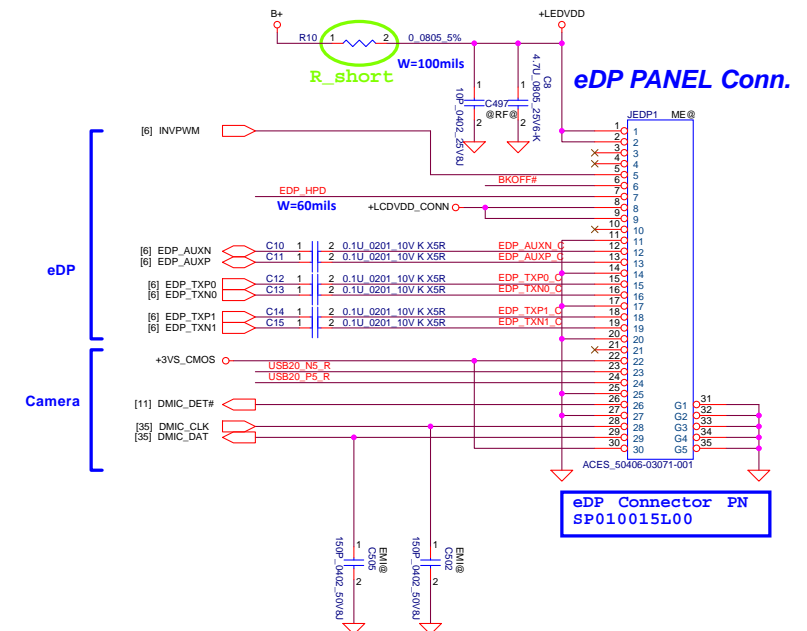
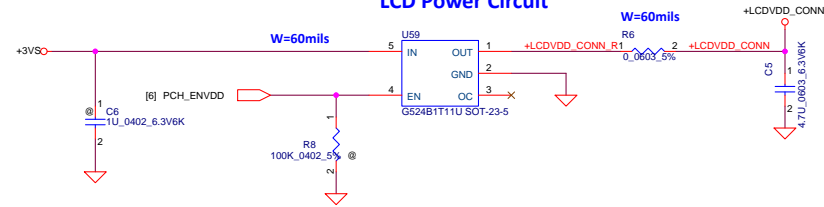
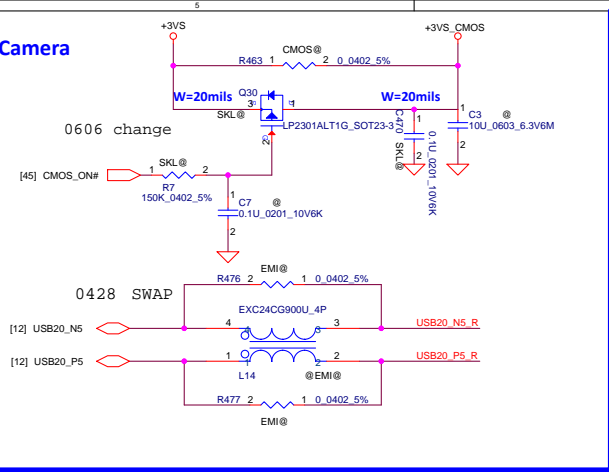
TPM 2.0

Layout Routing

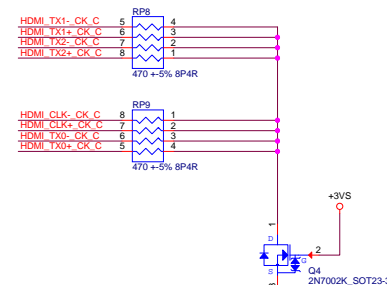
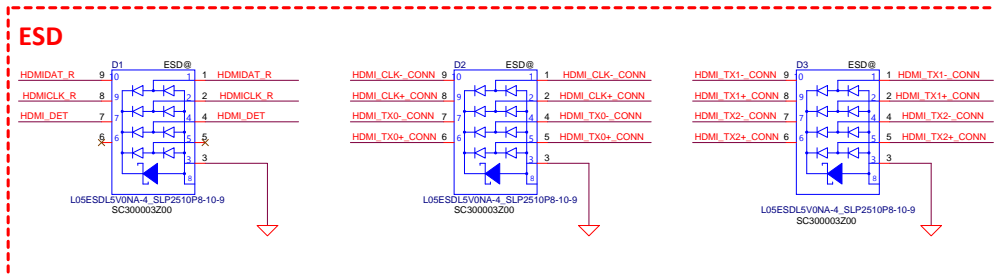
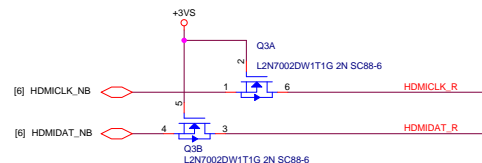
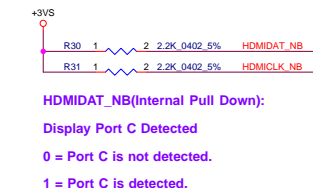
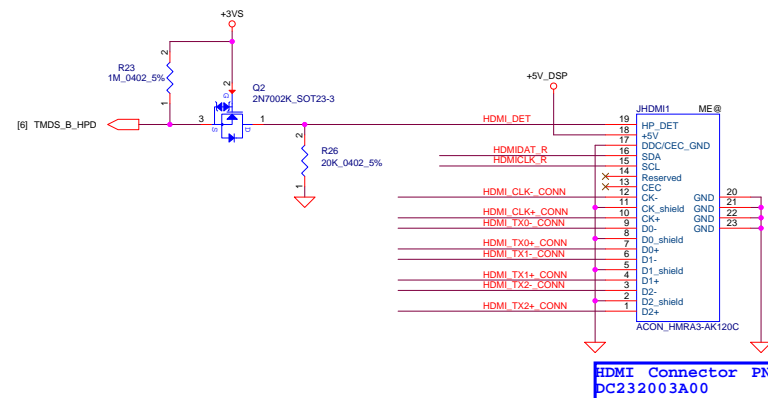
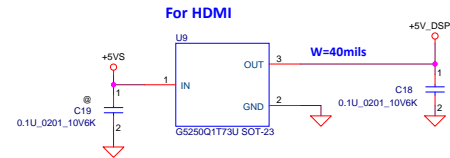
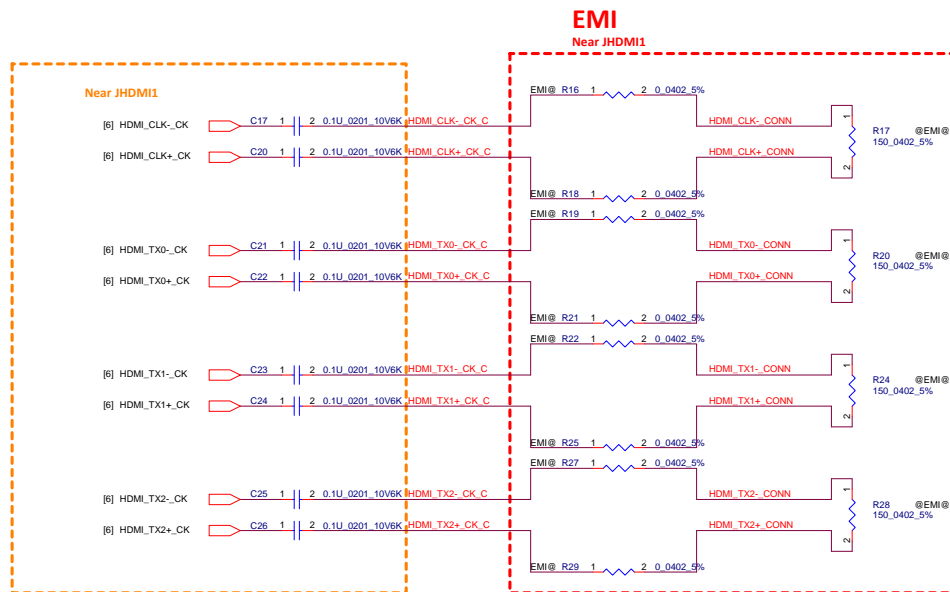


TPM/TCM Colay

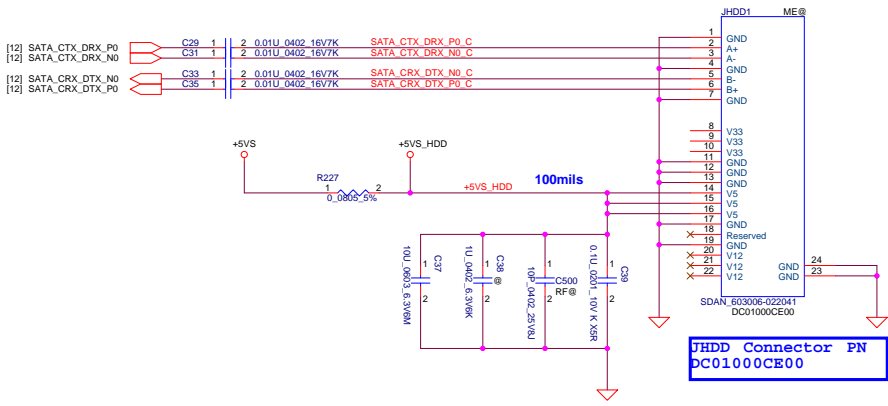
Nati or zInf i neon			Nati or zInf i neon		
TCM	TPM		TCM	TPM	
Pin1	NC	VDD	Pin17	NC	NC
Pin2	NC	GPIO	Pin18	LRESET#	LRESET#
Pin3	NC	NC	Pin19	LAD3	LAD3
Pin4	NC	NC	Pin20	VDD	VDD
Pin5	NC	NC	Pin21	LAD2	LAD2
Pin6	NC	NC	Pin22	LCLK	LCLK
Pin7	NC	NC	Pin23	LFRAME#	LFRAME#
Pin8	NC	NC	Pin24	LAD1	LAD1
Pin9	VDD	VDD	Pin25	VDD	VDD
Pin10	NC	VDD	Pin26	GND	GND
Pin11	GND	NC	Pin27	LAD0	LAD0
Pin12	NC	NC	Pin28	NC	SERIRQ
Pin13	NC	NC	Pin29	NC	NC
Pin14	NC	NC	Pin30	NC	NC
Pin15	NC	GND	Pin31	NC	PP
Pin16	GND	GND	Pin32	GND	GND

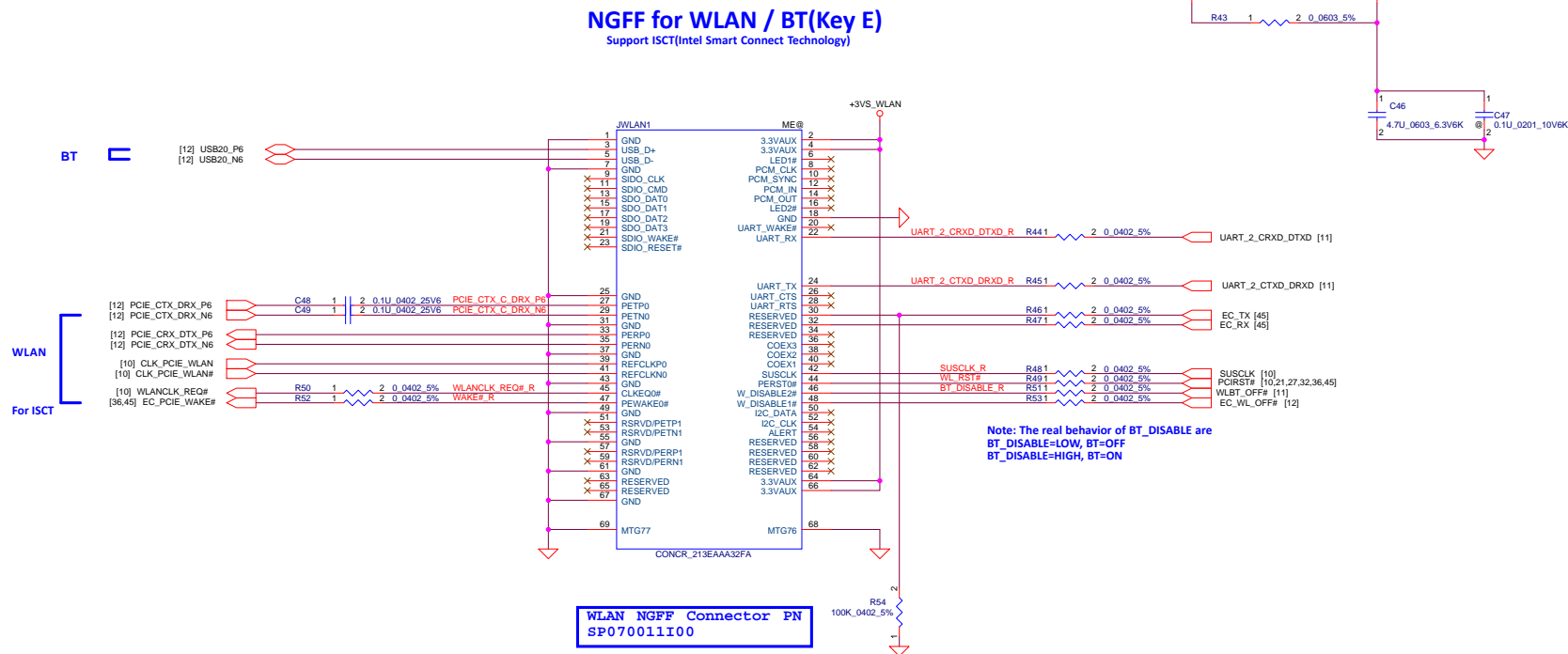


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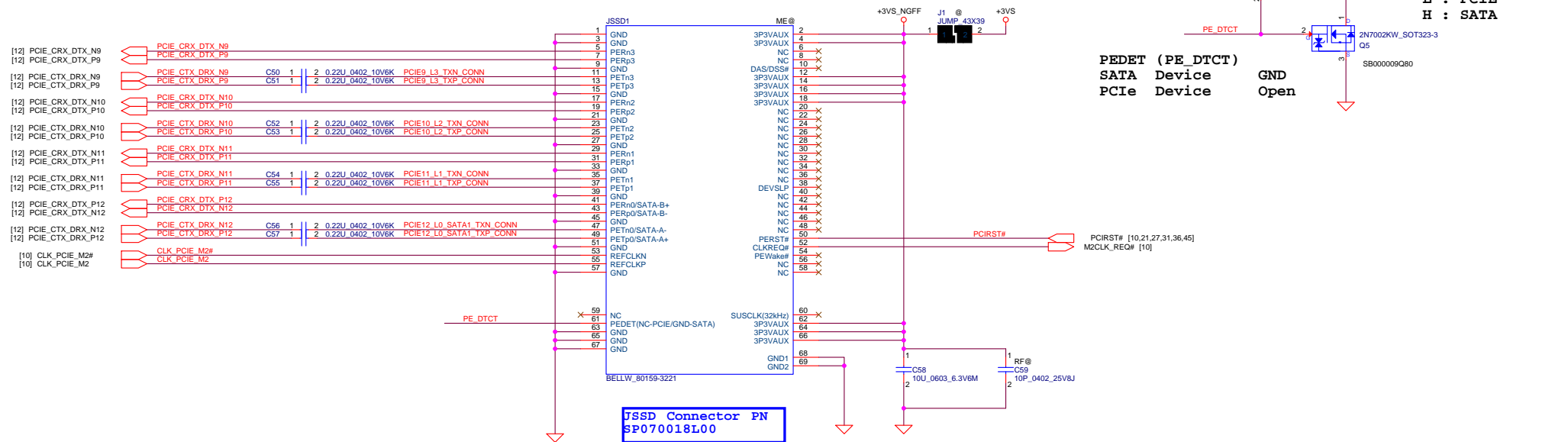


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Size		Document Number	LA-D562P	Rev 0.1
Date: Thursday, June 15, 2017		Sheet	29	of 66

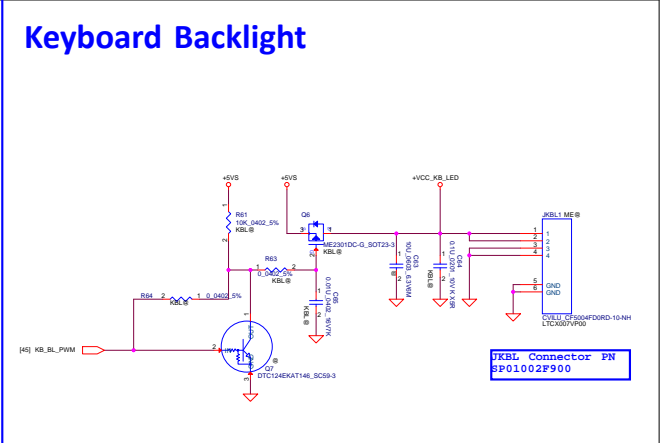
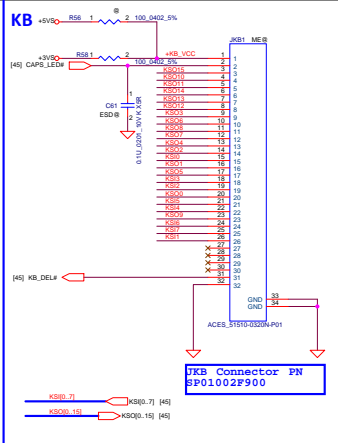
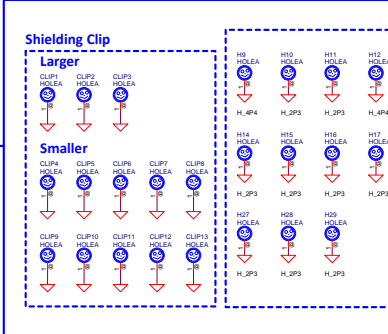
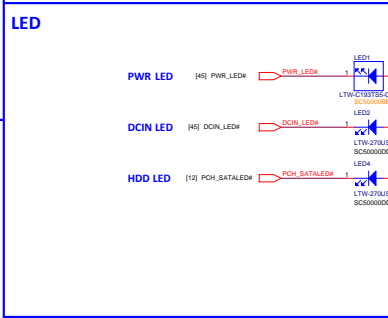
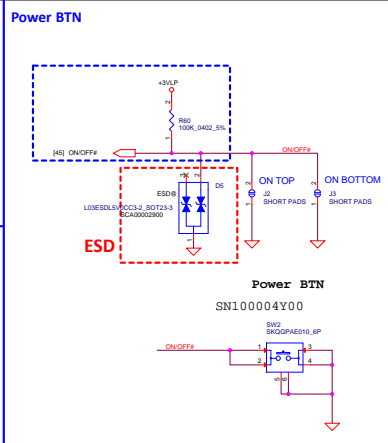
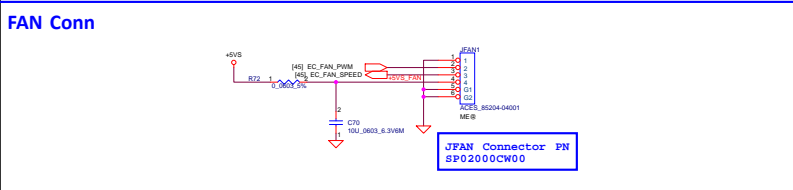
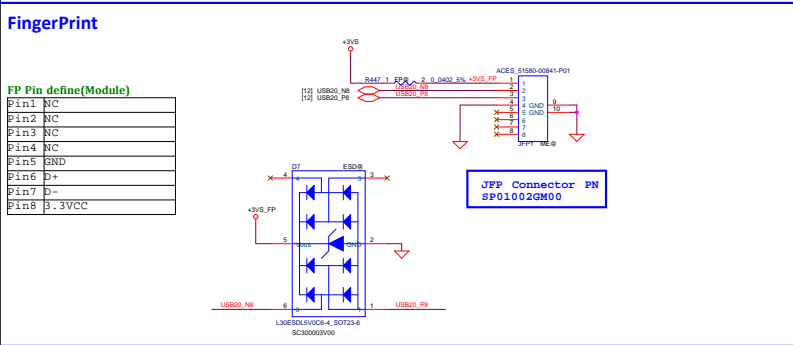
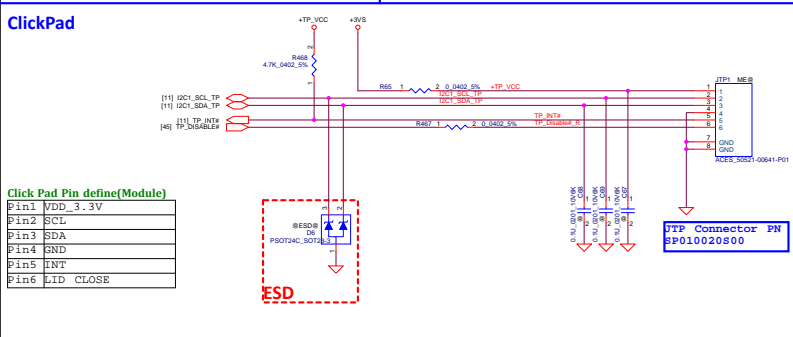
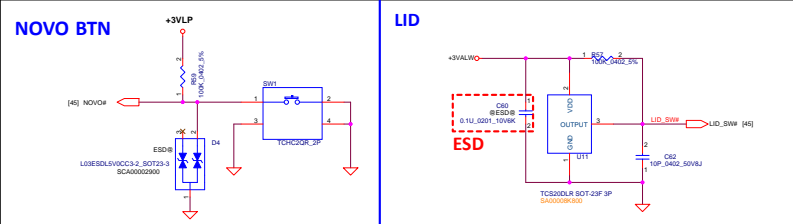




M.2 mSATA Conn

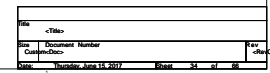


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				Date:	Thursday, June 15, 2017
				Sheet	32 of 66

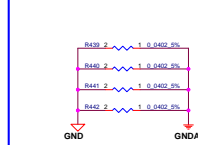
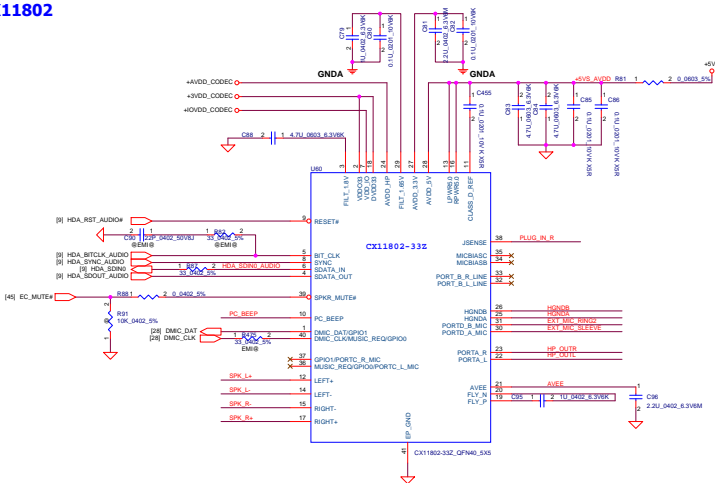


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Issued Date		2011/06/24		Deciphered Date		201207/12		Doc#	
2011/06/24		2011/06/24		201207/12		201207/12		LA-D562P	
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Rev		1.0		1.0		1.0		Rev	
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Date		Thursday, June 15, 2017		2017/06/15		2017/06/15		Rev	

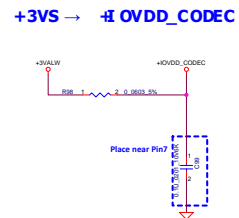
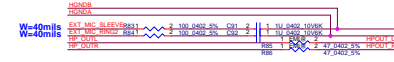
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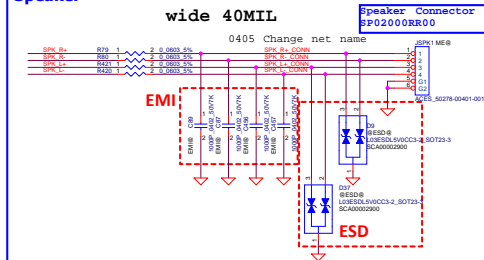
CX11802



Combo Jack



Speaker

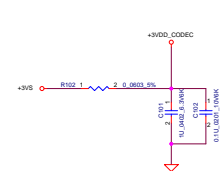
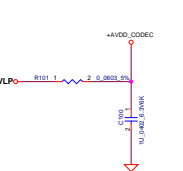


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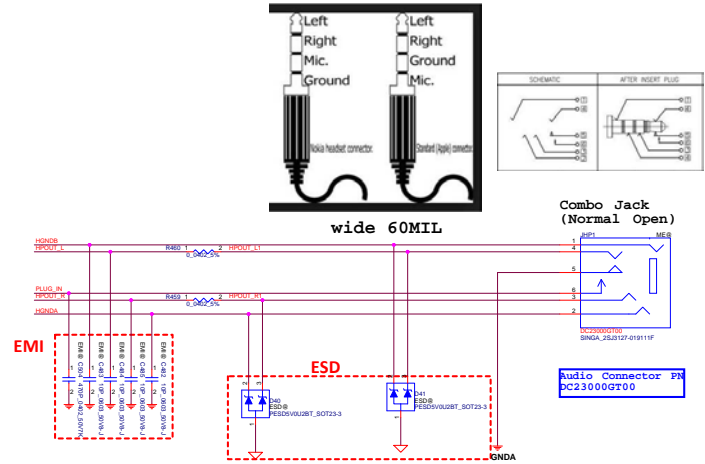
	+1.5VS	+1.8VS	+3VS	+5VS	+3V2WM
	1.5V(S0)	1.8V(S0)	3.3V(S0)	5V(S0)	3.3V(S0-S-8)
AMD Carrizo	V	V	V	V	V
AMD Carrizo-L	V	V	V	V	V
Intel Broadwell	V	V	V	V	V
Intel Haswell	V	V	V	V	V
Intel Skylake	V	V	V	V	V
Intel Bay trail-M				V	V

Each Platf or m HDA li nk Vdt age Support (R n 7):

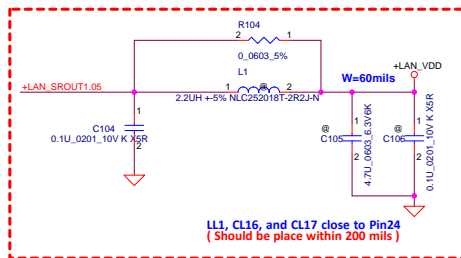
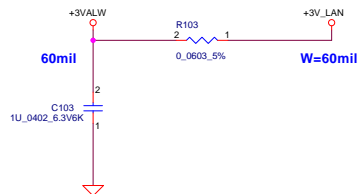
AMD Carrizo	3.3V	1.5V/1.8V
AMD Carrizo-L		V
Intel Broadwell	V	V
Intel Braswell		V
Intel Skylake	V	V
Intel Bay trail-M		V



PC Beep

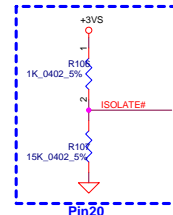
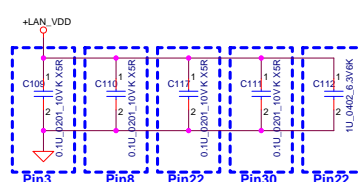
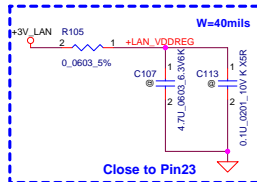
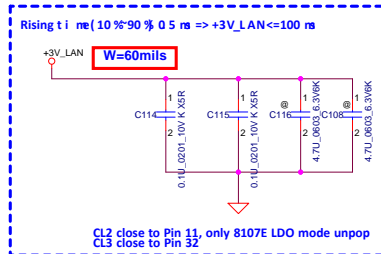


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Issued Date	2014/09/01	Deciphered Date	2016/09/01	File
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			Rev Count	0.1
MAY BE USED OR BE DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPEL ELECTRONICS, INC.			LA-D562P Issued: 04/14/2017 Rev: 04/14/2017	

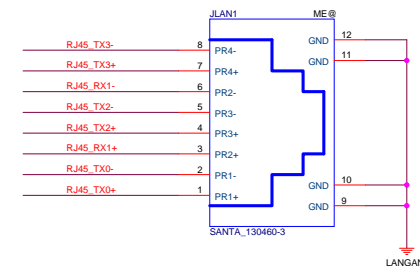


	1.0V Source	LL1	CL16, CL17	CL9, CL10	RL11	CL15
RTL8111H	LDO	X	X	X	O	O

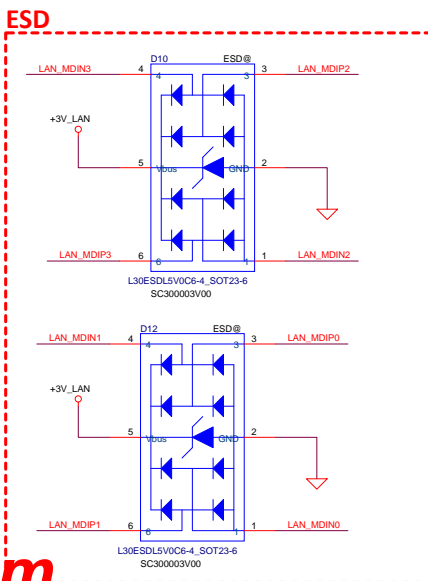
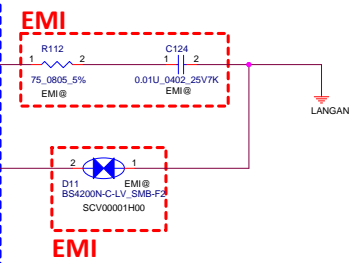
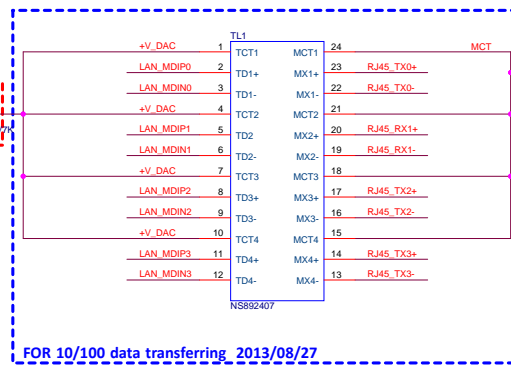
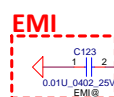
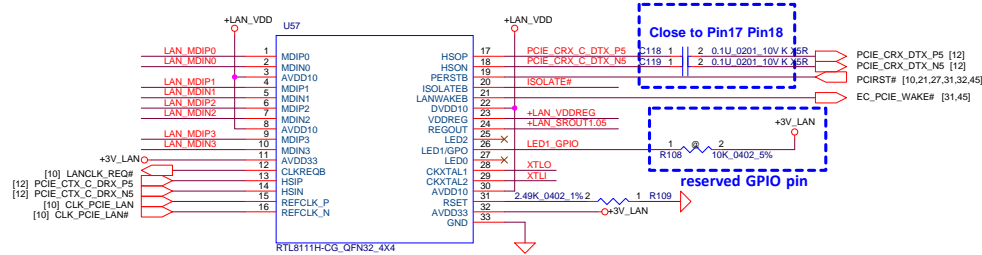
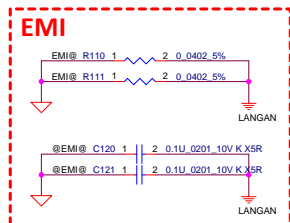
Please refer to the table above when using different 1.0V supply source.



RJ-45 CONN.

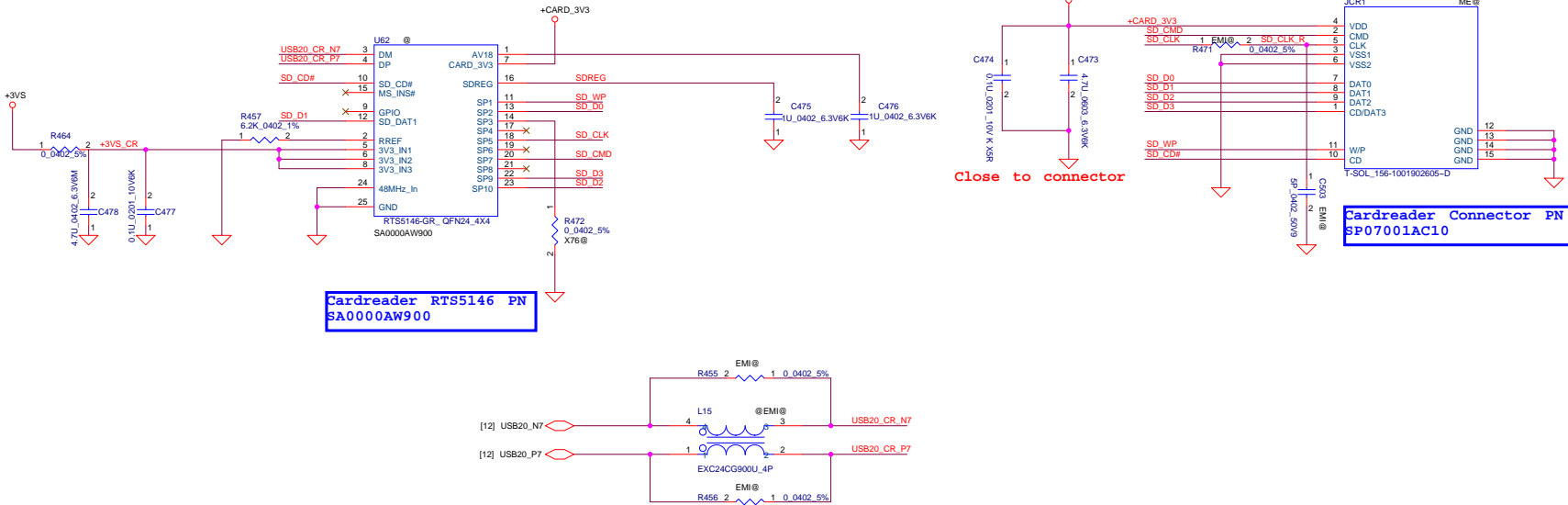


LAN Connector PIN DC23400DP00



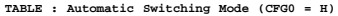
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Issued Date	2011/06/24	Rev 0.3
Deciphered Date	2012/07/12	LA-D061P
Title		LAN_RTL8111H / RTL8107E
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Card Reader



0329 move

Title <Title>			
Size Custom<Doc>	Document Number		Rev <Rev>Cdo>
Date: Thursday, June 15, 2017	Sheet	37 of 66	



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← LOGIC

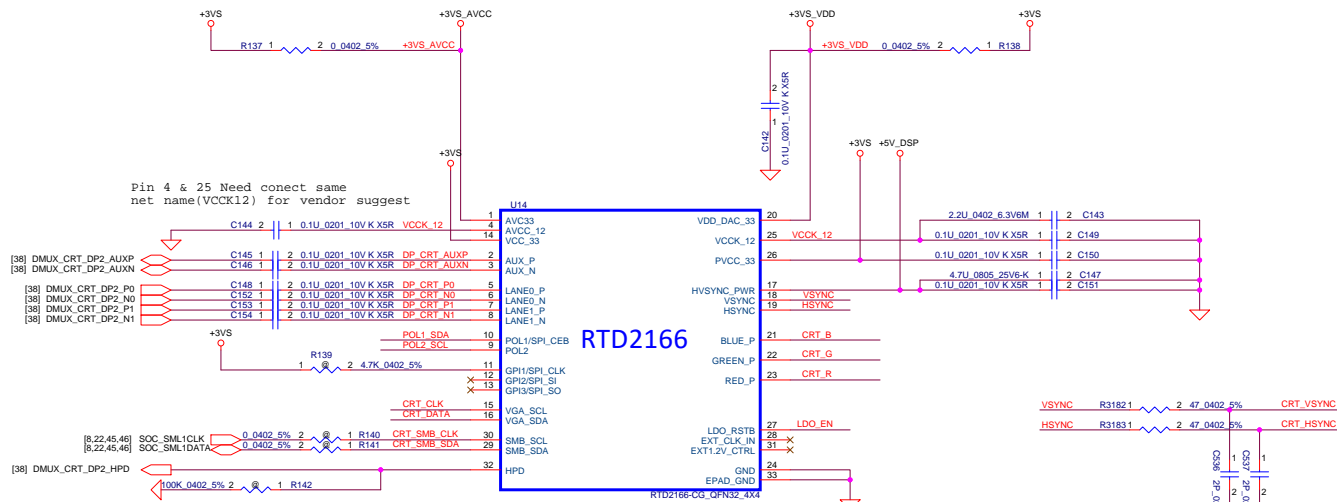
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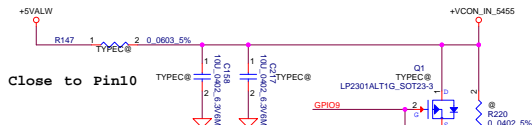
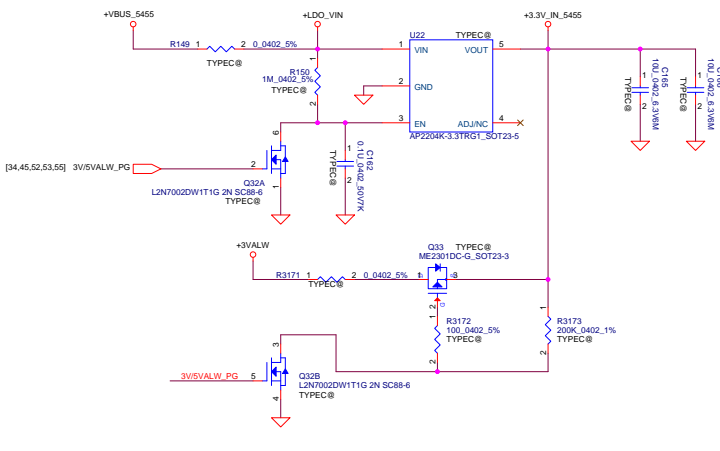
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				Drawn	Thursday, June 15, 2017	Sheet 38 of 66



dead battery

PD VIN 3.3V LDO



Close to Pin10

Support 3.3V IN version

From USB3.1

From DP MUX

TO SOC

SYMBOL
PD+MUX

Dead battery function Cfig. pin.
Tie to GND to disable dead battery 'Rd'.
Floating to enable dead battery 'Rd'.

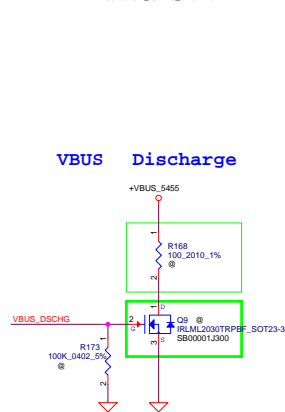
Realtek
RTS5455

100uA 3:2 MUX

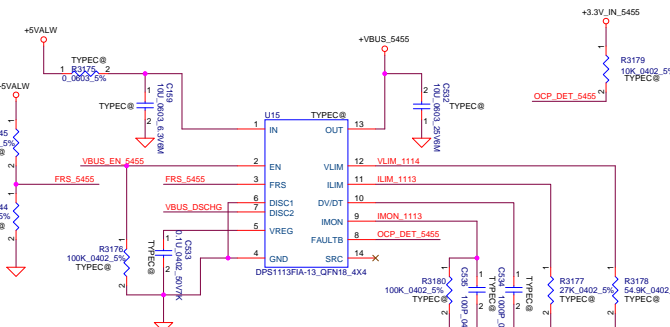
Low Speed MUX

RC1.2 8u11ch

VBUS Discharge



Close to USB typeC(JTYPEC2)



ISP Channel via USB Billboard

AUX_SBU1

AUX_SBU2

VBUS_DSCHG

FRS_5455

LOC_PWR_MON

OCDET_5455

LOC_PWR_MON

LOC_PWR_MON

LOC_PWR_MON

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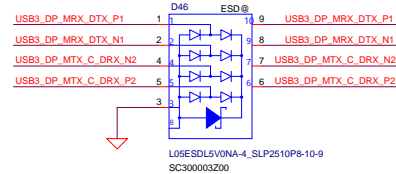
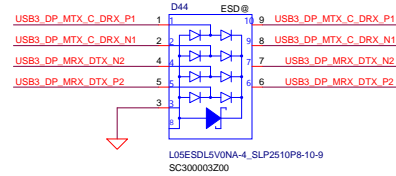
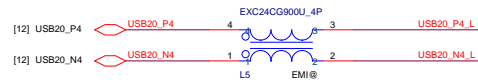
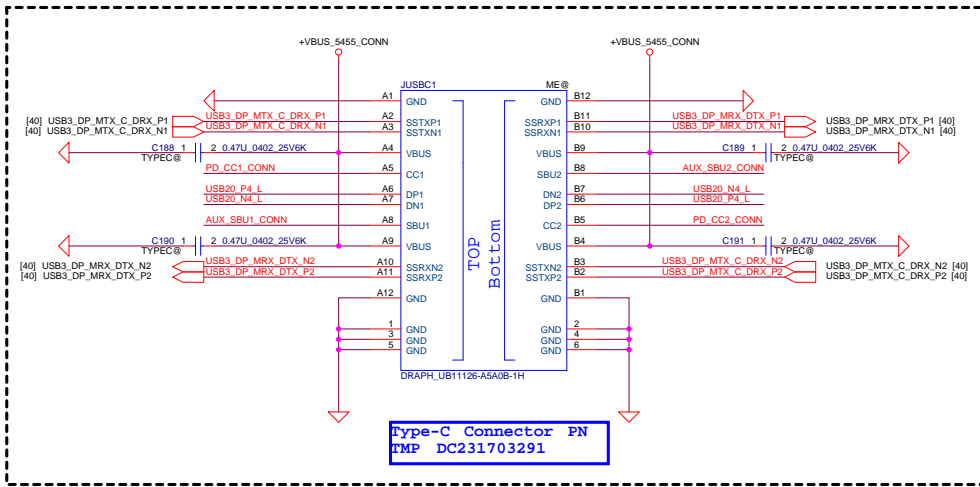
LOC_PWR_MON

LOC_PWR_MON

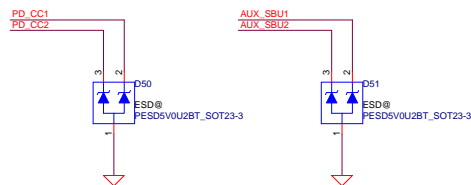
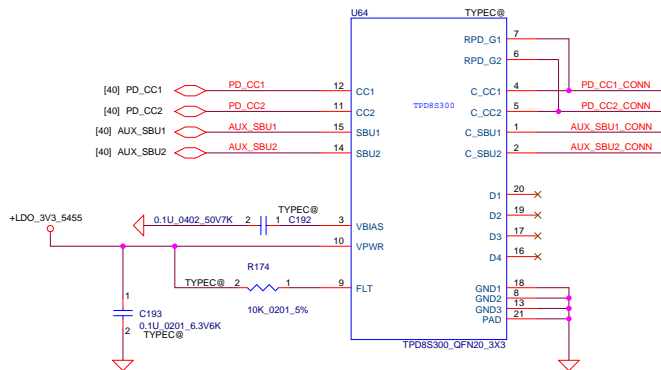
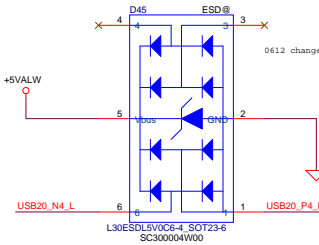
Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K

0314_Add
Connect 'LOC_PWR' net to local power for P/W to
decide if C port can become provider via PR_SMB.
Leave floating if no local power exists in the
system or in the application that 5455 can only
be powered on by local power.

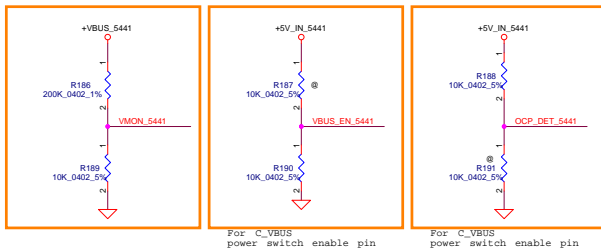
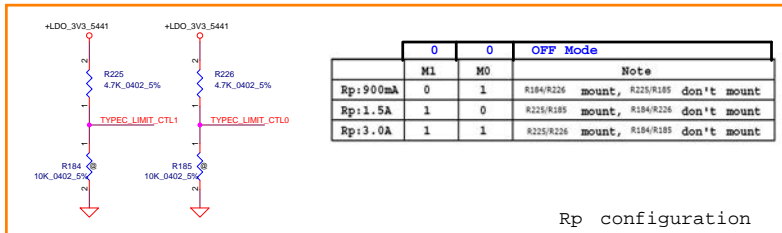
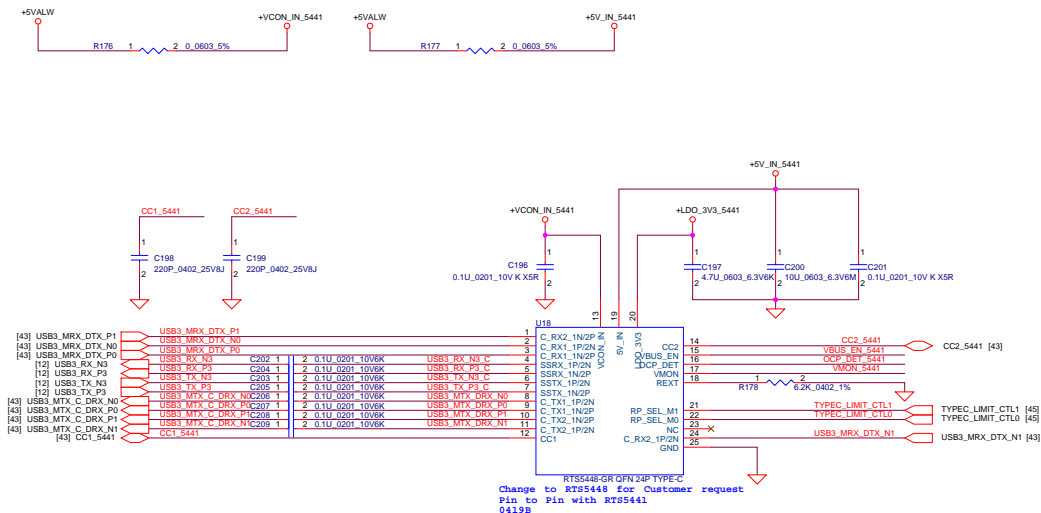
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Issued Date	Deciphered Date			
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Title: Compal Electronics, Inc. Type-C RTSS5455				
Revision: LA-E521P				
Date: Thursday, June 15, 2017				
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ESD for USB3 Lines and Control lines

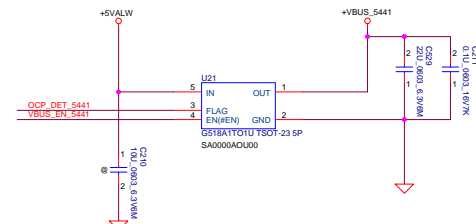


Security Classification	Compal Secret Data			Title	
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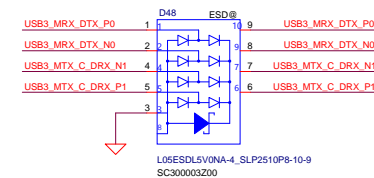
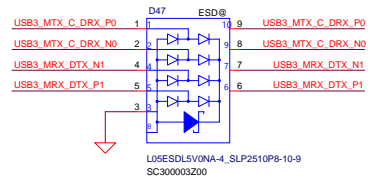
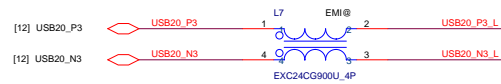
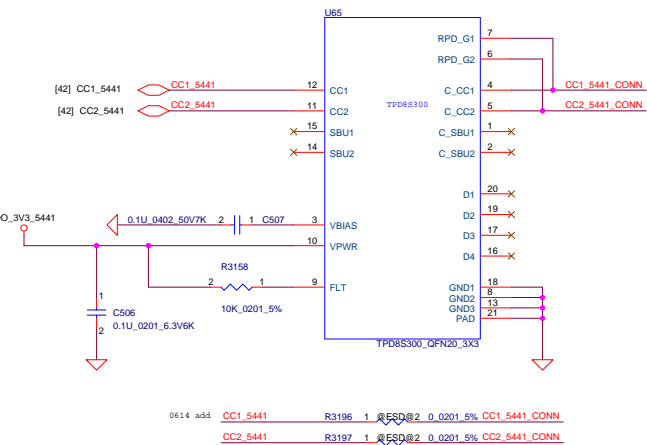
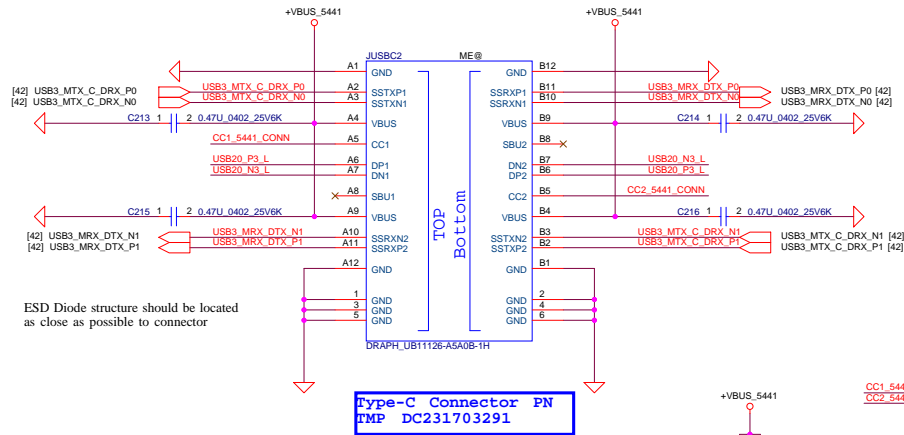


Power switch enable pin	Note	
Low Active	R190/R187 mount	Pull Up & Down
High Active	R190 mount, R187 don't mount	Pull Down

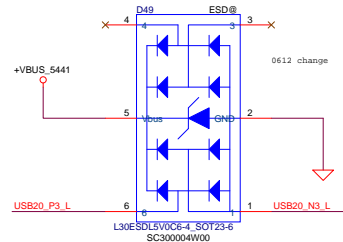
Power switch OCP pin	Note	
Low Active	R191/R188 mount	Pull Up & Down
High Active	R191 mount, R188 don't mount	Pull Down

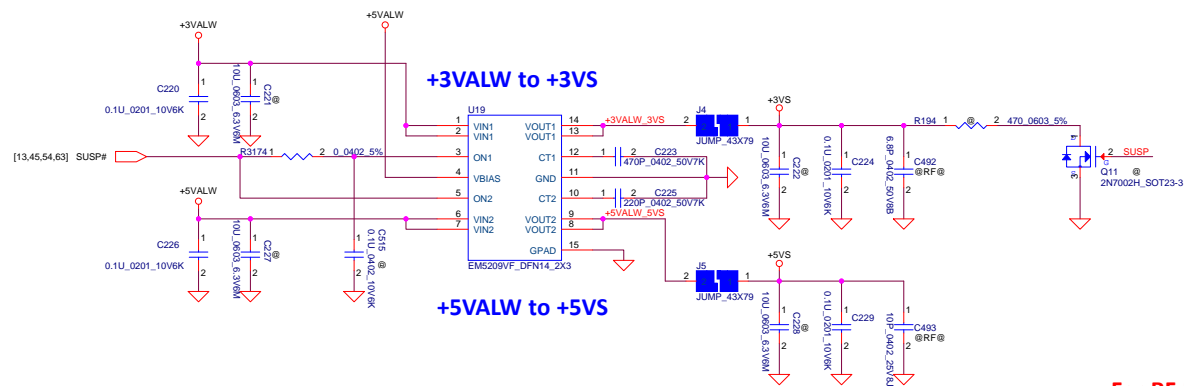


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Size	Document	Number	LA-C581P		
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Date:		Thursday, June 15, 2017		Sheet	42 of 63

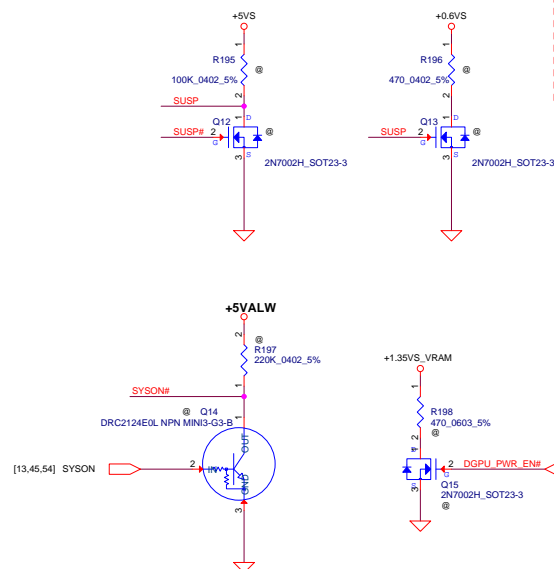
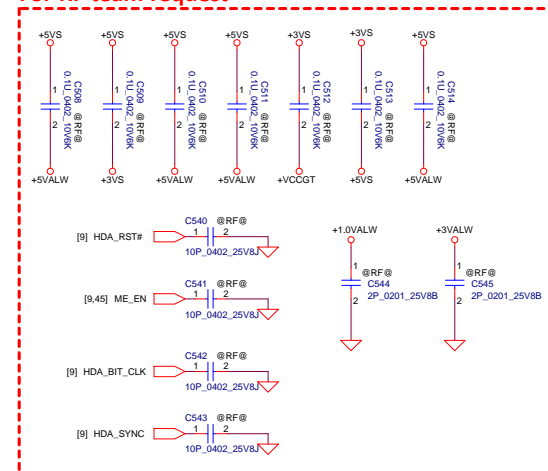


ESD for USB2 Lines and Control lines

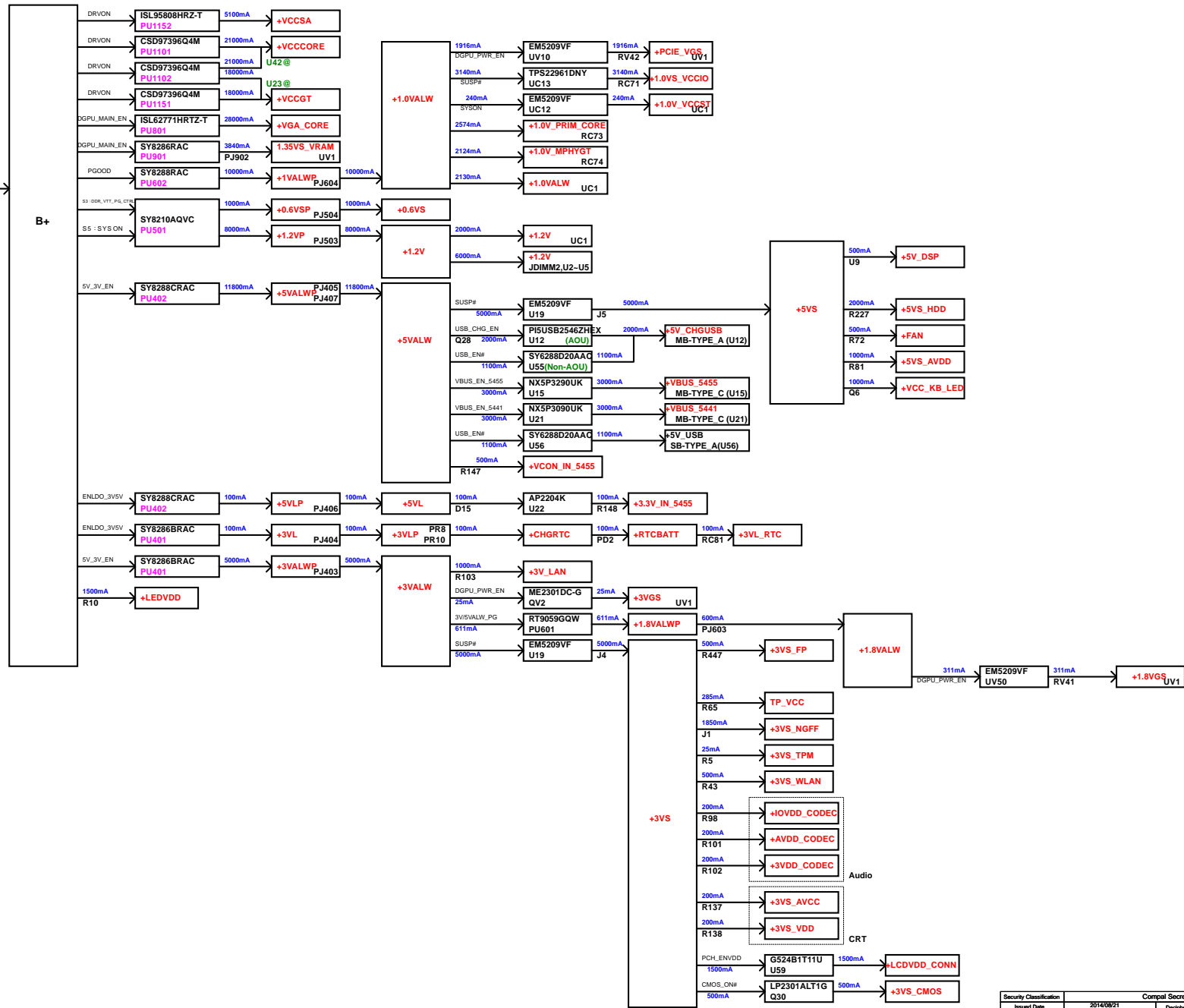
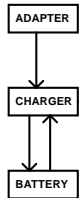




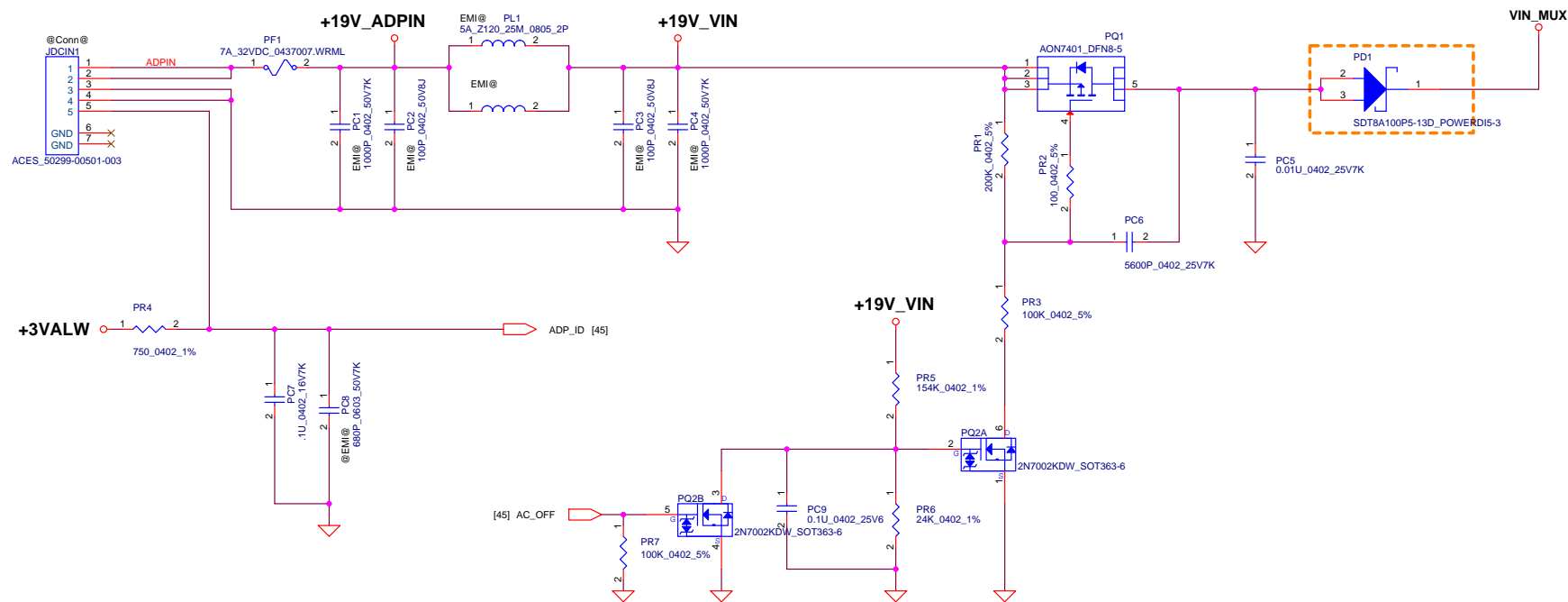
For RF team request



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2011/06/24		2012/07/12		DC Interface	
Size		Document Number		LA-D562P	
C		44		Rev 0.1	
Date: Thursday, June 15, 2017		Sheet		66	



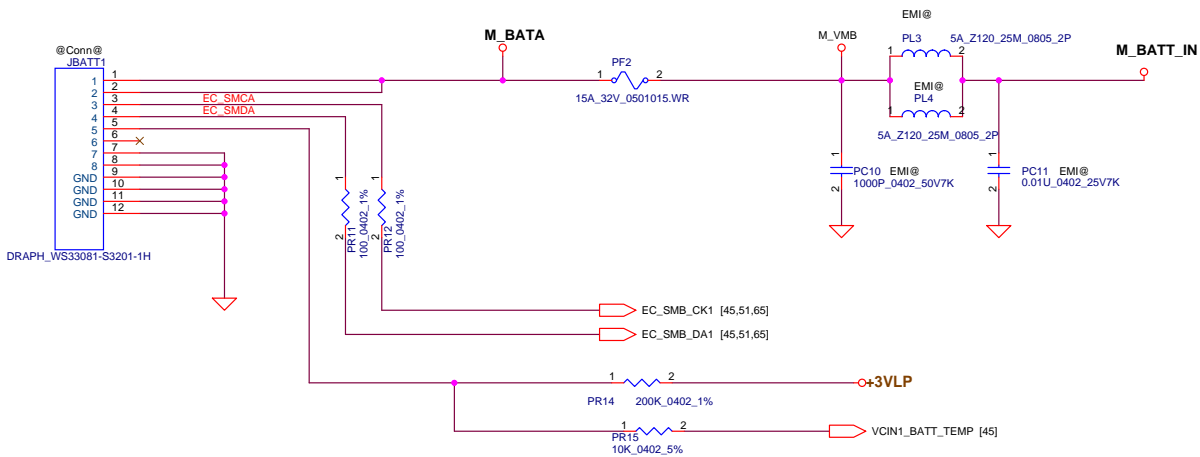
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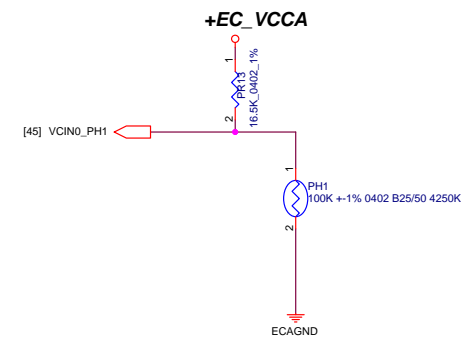
BOM Structure Table

Item	BOM Structure
For U22	U22@
For U23e	U23@
For U42	U42@
For DIS	VGA@
Support Type-C PD	PD@
For EMI	EMI@
For DIS of EMI	VGA_EMI@
For U23e of EMI	U23_EMI@
For U42 of EMI	U42_EMI@
For RF	RF@
For DIS of RF	VGA_RF@
For U23e of RF	U23_RF@
For U42 of RF	U42_RF@

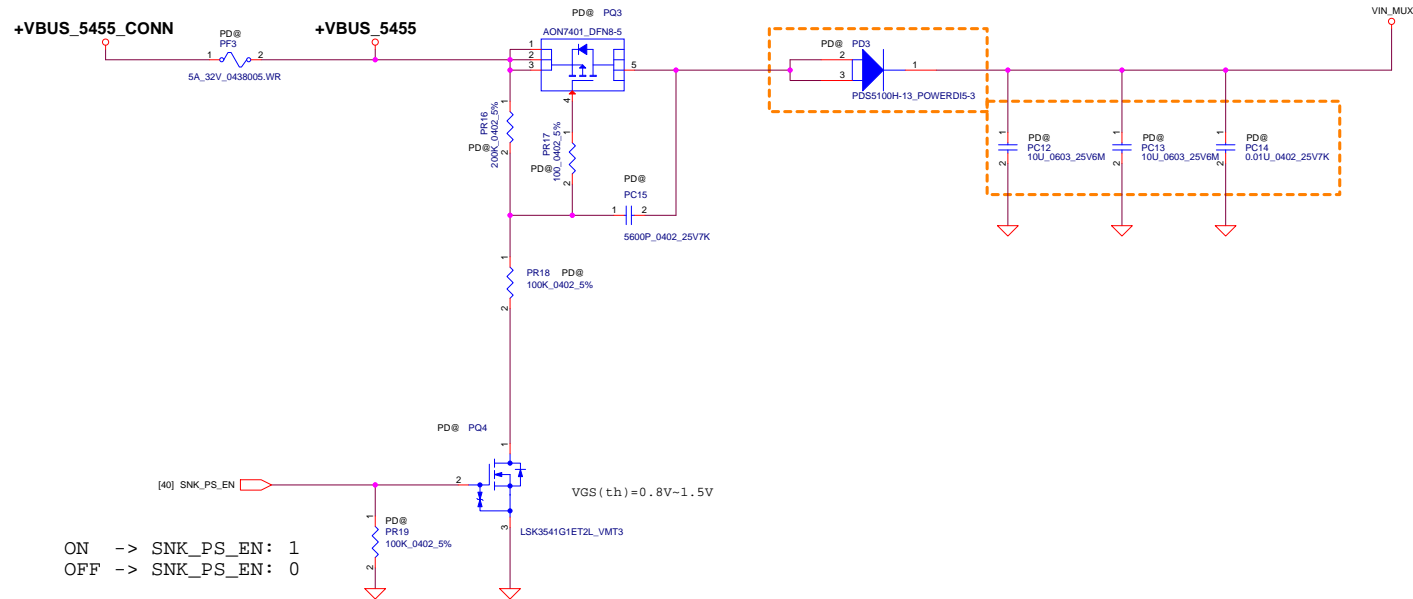
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PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

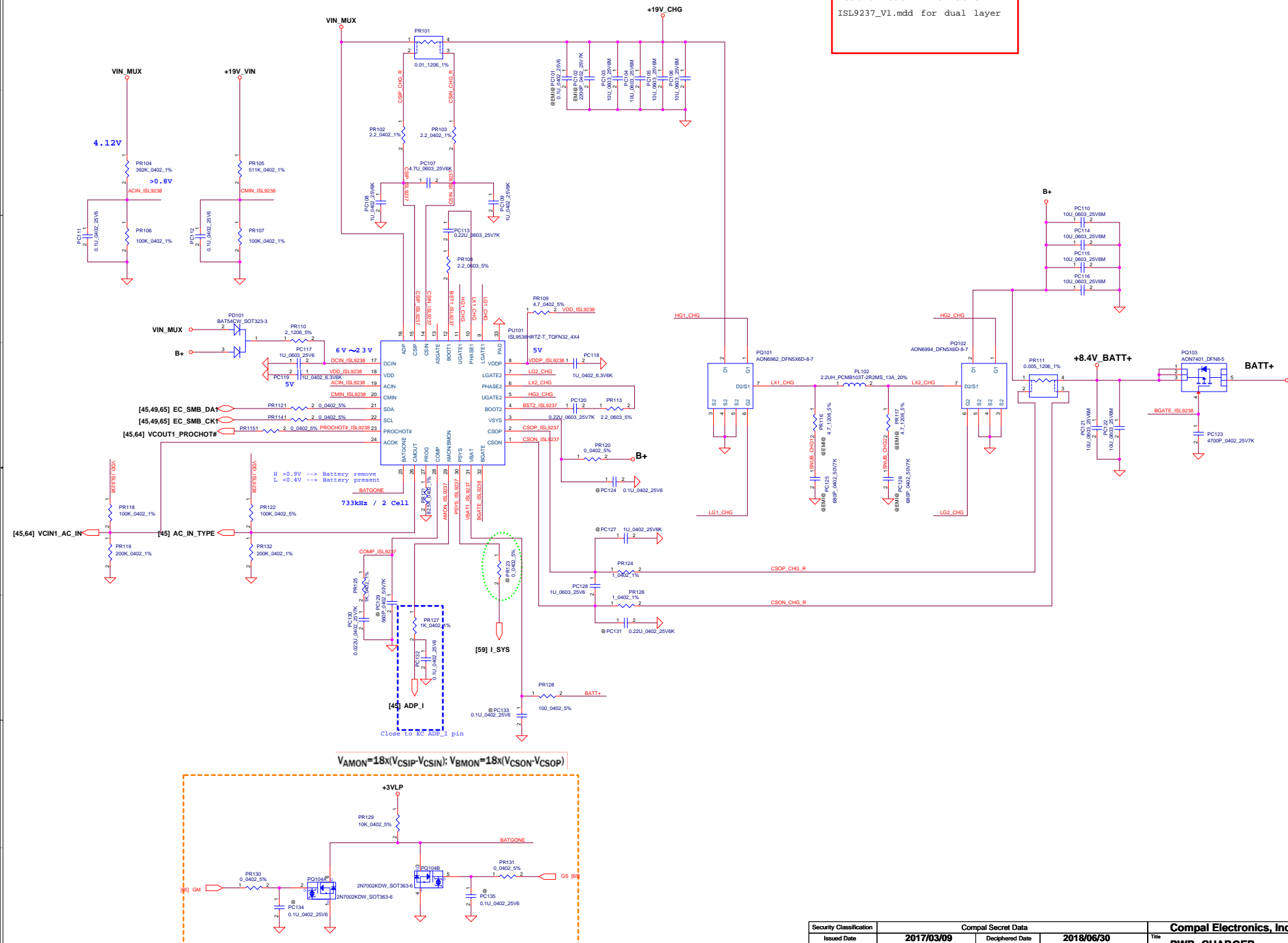


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								PWR-BATTERY CONN/OTP	
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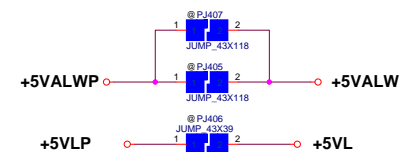
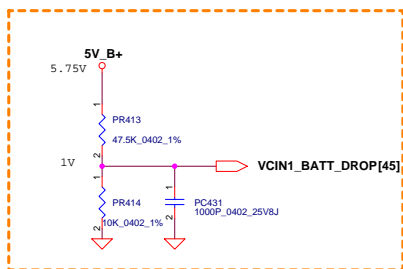


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Size	Document	Number	Rev	
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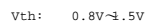
Module model information
ISL9237_V1.mdd for dual layer



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Size	Customer	Document Number	VE	Rev	0.1
Date: Thursday, June 15, 2017		Sheet: 61 of 68			

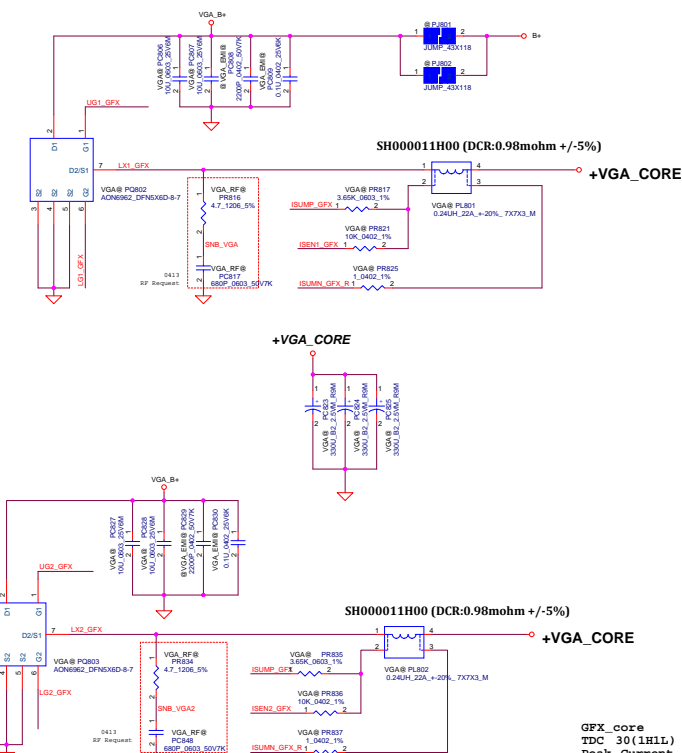


```
+5VALWP
Imax=10.5A,Ipeak=12.4A ;Fsw=300KHz
Iocp=(Rcs1*Itrip)/RdsOn
Rds : L/S -> typ:2.8mohm ; max: 3.5mohm
Itrip=9-11 uA
Iocp=16.49A
Output Cap. ESR=18mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.04A
```

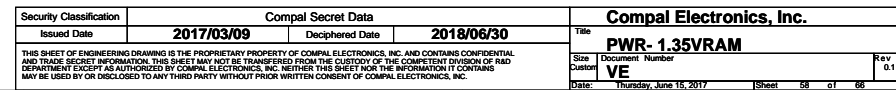


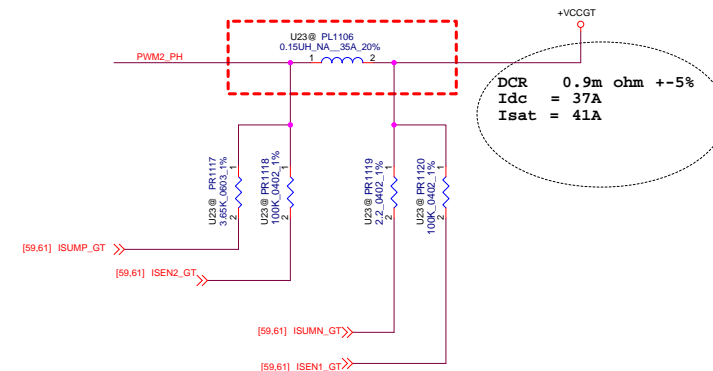
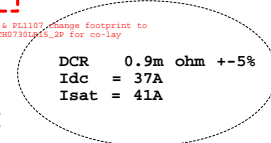
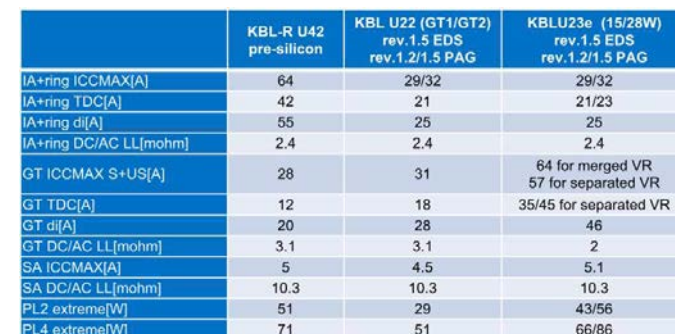
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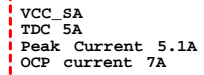
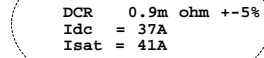
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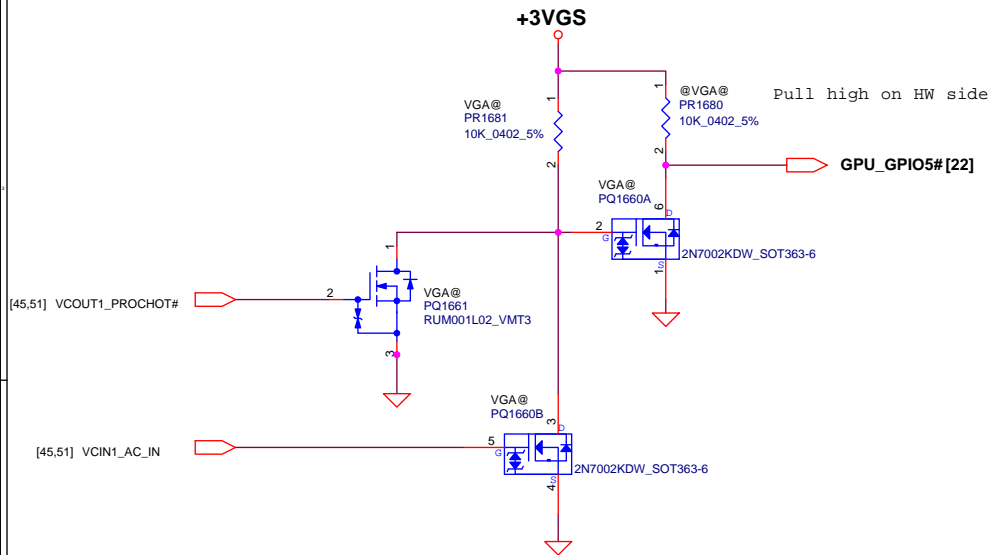
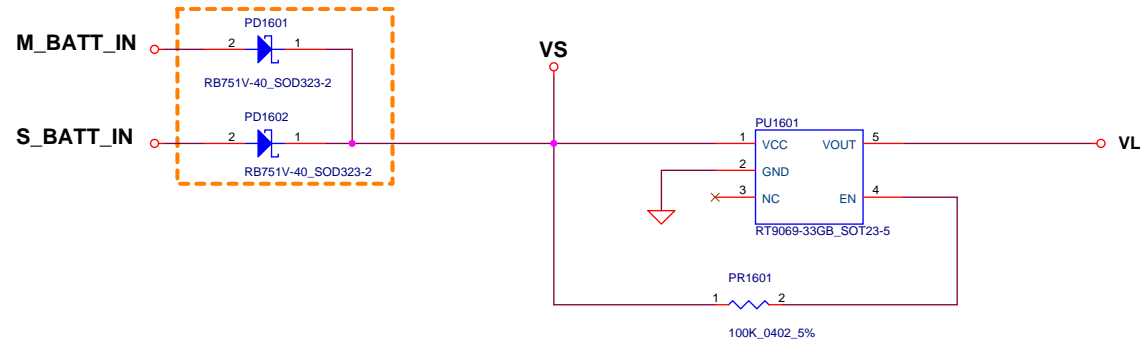
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Customer	DOWNR - Number		Rev	
VE			0.1	
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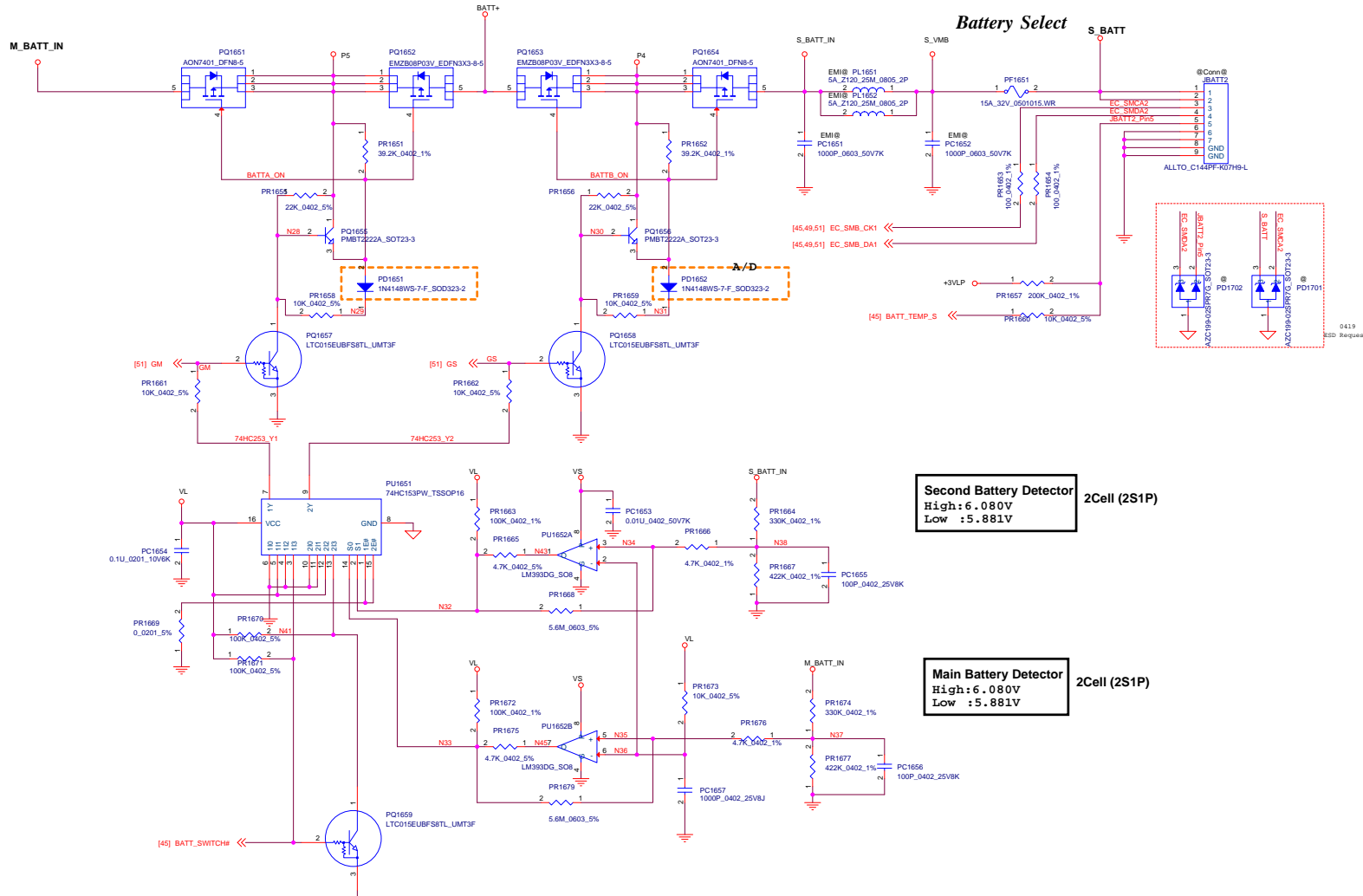




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BATT_SWITCH#
 High: M_BATT (A)
 Low : S_BATT (B)

Second Battery Detector
 High: 6.080V
 Low : 5.881V

2Cell (2S1P)

Main Battery Detector
 High: 6.080V
 Low : 5.881V

2Cell (2S1P)

Item	Reason for change	PG#	Modify List	Date	Phase
1		62	Change PR1201,PR1202,PR1203,PR1204 from 0.0002_0805_5% to SOLDER_PREFORMS_0402	0606A	SIV
2	Follow battery connector change	49	Change JBATT1 from SUYIN_125022HB008M200ZL to DRAPH_WS33081-S3201-1H	0606A	SIV
3	Adjust 1V voltage to meet ripple spec.	55	Change PR608 from 14.3K_0402_1% to 14K_0402_1%	0606A	SIV
4		64	Change PR1680.2 net from VGA_PROCHOT# to GPU_GPIO5#	0606A	SIV
5		60 61	1. Change PU1101,PU1102,PU1151 from CSD97396Q4M to AOZ5048QI 2. Change PC1101,PC1112,PC1151 from 1U_0603_10V6K to 4.7U_0603_10V6K	0606A	SIV
6		52 60 54 63 60 61	1. Change PC457 from SF000006500 to SF000006R00 2. Change PC1103,PC1104 from SF000006800 to SF000007200 3. Change PL501 from SH00000BJ00 to SH00000YE00 4. Change PL1501 from SH00000UE00 to SH00000Z300 5. Change PL1101,PL1105,PL1106,PL1151 from SH00000X700 to SH00001EF00 6. Change PL1153 from SH00001SM00 to SH00001ED00	0606A	SIV
7		57	Change PU801.4 netname from GPU_PROCHOT# to GPU_VRHOT#	0607B	SIV
8	HW request. Avoid +1VALW turn on twice.	55	Change PU601 PGood pull high from +3VALW to +1.8ALWP	0609A	SIV
9		62	Reserve 220u D7 4.5mohm poscap on +VCCORE and +VCCGT power rails (PC1658,PC1659)	0612A	SIV
10		55 58 63	1. Add PC620 for +1VALW input cap 2. Add PC914 for +1.35VGSP input cap 3. Add PC1511 for +1.0VS_VCCOPCP input cap	0612A	SIV
11		64	1. Change PD1601 from 1N4148WS-7-F_SOD323-2 to RB751V-40_SOD323-2 2. Delete PQ1601,PR1602,PD1603	0614A	SIV
12	For HW sequence request.	58	1. PR902 change from 0 to 88.7K 2. PC902 change to 0.1uF and pop.	0614B	SIV
13	During EC autoloading, need turn on power LED	53	Add PR461 for pull high 5VLDO_EN to +3VLP	0614B	SIV

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